Netra™ CP2300 cPSB Board Installation and Technical Reference Manual

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www.sun.com

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Safety Agency Compliance Statements

Read this section before beginning any procedure. The following text provides safety precautions to follow when installing a Sun Microsystems product.

Safety Precautions

For your protection, observe the following safety precautions when setting up your equipment:

- Follow all cautions and instructions marked on the equipment.
- Ensure that the voltage and frequency of your power source match the voltage and frequency inscribed on the equipment's electrical rating label.
- Never push objects of any kind through openings in the equipment. Dangerous voltages may be present. Conductive foreign objects could produce a short circuit that could cause fire, electric shock, or damage to your equipment.

Symbols

The following symbols may appear in this book:

Caution – There is a risk of personal injury and equipment damage. Follow the instructions.

Caution – Hot surface. Avoid contact. Surfaces are hot and may cause personal injury if touched.

Caution – Hazardous voltages are present. To reduce the risk of electric shock and danger to personal health, follow the instructions.

Depending on the type of power switch your device has, one of the following symbols may be used:

On – Applies AC power to the system.

Off – Removes AC power from the system.

Standby – The On/Standby switch is in the standby position.

Modifications to Equipment

Do not make mechanical or electrical modifications to the equipment. Sun Microsystems is not responsible for regulatory compliance of a modified Sun product.

Placement of a Sun Product

Caution – Do not block or cover the openings of your Sun product. Never place a Sun product near a radiator or heat register. Failure to follow these guidelines can cause overheating and affect the reliability of your Sun product.

Noise Level

In compliance with the requirements defined in DIN 45635 Part 1000, the workplace-dependent noise level of this product is less than 70 db(A).

SELV Compliance

Safety status of I/O connections comply to SELV requirements.

Power Cord Connection

Caution – Sun products are designed to work with power systems having a grounded neutral (grounded return for DC-powered products). To reduce the risk of electric shock, do not plug Sun products into any other type of power system. Contact your facilities manager or a qualified electrician if you are not sure what type of power is supplied to your building.

Caution – Not all power cords have the same current ratings. Household extension cords do not have overload protection and are not meant for use with computer systems. Do not use household extension cords with your Sun product.

The following caution applies only to devices with a Standby power switch:

Caution – The power switch of this product functions as a standby type device only. The power cord serves as the primary disconnect device for the system. Be sure to plug the power cord into a grounded power outlet that is nearby the system and is readily accessible. Do not connect the power cord when the power supply has been removed from the system chassis.

The following caution applies only to devices with multiple power cords:

Caution – For products with multiple power cords, all power cords must be disconnected to completely remove power from the system.

Battery Warning

Caution – There is danger of explosion if batteries are mishandled or incorrectly replaced. On systems with replaceable batteries, replace only with the same manufacturer and type or equivalent type recommended by the manufacturer per the instructions provided in the product service manual. Do not disassemble batteries or attempt to recharge them outside the system. Do not dispose of batteries in fire. Dispose of batteries properly in accordance with the manufacturer's instructions and local regulations. Note that on Sun CPU boards, there is a lithium battery molded into the real-time clock. These batteries are not customer replaceable parts.

System Unit Cover

You must remove the cover of your Sun computer system unit to add cards, memory, or internal storage devices. Be sure to replace the cover before powering on your computer system.

Caution – Do not operate Sun products without the cover in place. Failure to take this precaution may result in personal injury and system damage.

Rack System Warning

The following warnings apply to Racks and Rack Mounted systems.

Caution – For safety, equipment should always be loaded from the bottom up. That is, install the equipment that will be mounted in the lowest part of the rack first, then the next higher systems, etc.

Caution – To prevent the rack from tipping during equipment installation, the anti-tilt bar on the rack must be deployed.

Caution – To prevent extreme operating temperature within the rack insure that the maximum temperature does not exceed the product's ambient rated temperatures.

Caution – To prevent extreme operating temperatures due to reduced airflow consideration should be made to the amount of air flow that is required for a safe operation of the equipment.

Laser Compliance Notice

Sun products that use laser technology comply with Class 1 laser requirements.

Class 1 Laser Product
Luokan 1 Laserlaite
Klasse 1 Laser Apparat
Laser Klasse 1

CD and DVD Devices

The following caution applies to CD, DVD, and other optical devices.

Caution – Use of controls, adjustments, or the performance of procedures other than those specified herein may result in hazardous radiation exposure.

Conformité aux normes de sécurité

Veuillez lire attentivement cette section avant de commencer. Ce texte traite des mesures de sécurité qu'il convient de prendre pour l'installation d'un produit Sun Microsystems.

Mesures de sécurité

Pour votre sécurité, nous vous recommandons de suivre scrupuleusement les mesures de sécurité ci-dessous lorsque vous installez votre matériel:

- Suivez tous les avertissements et toutes les instructions inscrites sur le matériel.
- Assurez-vous que la tension et la fréquence de votre source d'alimentation correspondent à la tension et à la fréquence indiquées sur l'étiquette de la tension électrique nominale du matériel
- N'introduisez jamais d'objets quels qu'ils soient dans les ouvertures de l'équipement. Vous pourriez vous trouver en présence de hautes tensions dangereuses. Tout objet étranger conducteur risque de produire un court-circuit pouvant présenter un risque d'incendie ou de décharge électrique, ou susceptible d'endommager le matériel.

Symboles

Vous trouverez ci-dessous la signification des différents symboles utilisés:

Attention – Vous risquez d'endommager le matériel ou de vous blesser. Veuillez suivre les instructions.

Attention – Surfaces brûlantes. Evitez tout contact. Les surfaces sont brûlantes. Vous risquez de vous blesser si vous les touchez.

Attention – Tensions dangereuses. Pour réduire les risques de décharge électrique et de danger physique, observez les consignes indiquées.

Selon le type d'interrupteur marche / arrêt dont votre appareil est équipé, l'un des symboles suivants sera utilisé:

Marche – Met le système sous tension alternative.

Arret – Met le système hors tension alternative.

Veilleuse – L'interrupteur Marche / Veille est sur la position de veille.

Modification du matériel

N'apportez aucune modification mécanique ou électrique au matériel. Sun Microsystems décline toute responsabilité quant à la non-conformité éventuelle d'un produit Sun modifié.

Positionnement d'un produit Sun

Attention – Evitez d'obstruer ou de recouvrir les orifices de votre produit Sun. N'installez jamais un produit Sun près d'un radiateur ou d'une source de chaleur. Si vous ne respectez pas ces consignes, votre produit Sun risque de surchauffer et son fonctionnement en sera altéré.

Niveau de pression acoustique

Le niveau de pression acoustique du lieu de travail définie par la norme DIN 45 635 Part 1000 doit être au maximum de 70 db(A).

Conformité SELV

Le niveau de sécurité des connexions E / S est conforme aux normes SELV.

Connexion du cordon d'alimentation

Attention – Les produits Sun sont conçus pour fonctionner avec des systèmes d'alimentation équipés d'un conducteur neutre relié à la terre (conducteur neutre pour produits alimentés en CC). Pour réduire les risques de décharge électrique, ne branchez jamais les produits Sun sur une source d'alimentation d'un autre type. Contactez le gérant de votre bâtiment ou un électricien agréé si vous avez le moindre doute quant au type d'alimentation fourni dans votre bâtiment.

Attention – Tous les cordons d'alimentation ne présentent pas les mêmes caractéristiques électriques. Les cordons d'alimentation à usage domestique ne sont pas protégés contre les surtensions et ne sont pas conçus pour être utilisés avec des ordinateurs. N'utilisez jamais de cordon d'alimentation à usage domestique avec les produits Sun.

L'avertissement suivant s'applique uniquement aux systèmes équipés d'un interrupteur Veille:

Attention – L'interrupteur d'alimentation de ce produit fonctionne uniquement comme un dispositif de mise en veille. Le cordon d'alimentation constitue le moyen principal de déconnexion de l'alimentation pour le système. Assurez-vous de le brancher dans une prise d'alimentation mise à la terre près du système et facile d'accès. Ne le branchez pas lorsque l'alimentation électrique ne se trouve pas dans le châssis du système.

L'avertissement suivant s'applique uniquement aux systèmes équipés de plusieurs cordons d'alimentation:

Attention – Pour mettre un système équipé de plusieurs cordons d'alimentation hors tension, il est nécessaire de débrancher tous les cordons d'alimentation.

Mise en garde relative aux batteries

Attention – Les batteries risquent d’exploser en cas de manipulation maladroite ou de remplacement incorrect. Pour les systèmes dont les batteries sont remplaçables, effectuez les remplacements uniquement selon le modèle du fabricant ou un modèle équivalent recommandé par le fabricant, conformément aux instructions fournies dans le manuel de service du système. N’essayez en aucun cas de démonter les batteries, ni de les recharger hors du système. Ne les jetez pas au feu. Mettez-les au rebut selon les instructions du fabricant et conformément à la législation locale en vigueur. Notez que sur les cartes processeur de Sun, une batterie au lithium a été moulée dans l'horloge temps réel. Les batteries ne sont pas des pièces remplaçables par le client.

Couvercle de l'unité

Pour ajouter des cartes, de la mémoire ou des périphériques de stockage internes, vous devez retirer le couvercle de votre système Sun. Remettez le couvercle supérieur en place avant de mettre votre système sous tension.

Attention – Ne mettez jamais des produits Sun sous tension si leur couvercle supérieur n'est pas mis en place. Si vous ne prenez pas ces précautions, vous risquez de vous blesser ou d'endommager le système.

Mise en garde relative au système en rack

La mise en garde suivante s'applique aux racks et aux systèmes montés en rack.

Attention – Pour des raisons de sécurité, le matériel doit toujours être chargé du bas vers le haut. En d'autres termes, vous devez installer, en premier, le matériel qui doit se trouver dans la partie la plus inférieure du rack, puis installer le matériel sur le niveau suivant, etc.

Attention – Afin d'éviter que le rack ne penche pendant l'installation du matériel, tirez la barre anti-basculement du rack.

Attention – Pour éviter des températures de fonctionnement extrêmes dans le rack, assurez-vous que la température maximale ne dépasse pas la fourchette de températures ambiantes du produit déterminée par le fabricant.

Attention – Afin d'empêcher des températures de fonctionnement extrêmes provoquées par une aération insuffisante, assurez-vous de fournir une aération appropriée pour un fonctionnement du matériel en toute sécurité

Avis de conformité des appareils laser

Les produits Sun qui font appel aux technologies lasers sont conformes aux normes de la classe 1 en la matière.

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Périphériques CD et DVD

L'avertissement suivant s'applique aux périphériques CD, DVD et autres périphériques optiques:

Attention – L'utilisation de contrôles et de réglages ou l'application de procédures autres que ceux spécifiés dans le présent document peuvent entraîner une exposition à des radiations dangereuses.

Einhaltung sicherheitsbehördlicher Vorschriften

Lesen Sie vor dem Ausführen von Arbeiten diesen Abschnitt. Im folgenden Text werden Sicherheitsvorkehrungen beschrieben, die Sie bei der Installation eines Sun Microsystems-Produkts beachten müssen.

Sicherheitsvorkehrungen

Treffen Sie zu Ihrem eigenen Schutz bei der Installation des Geräts die folgenden Sicherheitsvorkehrungen:

- Beachten Sie alle auf den Geräten angebrachten Warnhinweise und Anweisungen.
- Stellen Sie sicher, dass Spannung und Frequenz der Stromversorgung den Nennleistungen auf dem am Gerät angebrachten Etikett entsprechen.
- Führen Sie niemals Fremdobjekte in die Öffnungen am Gerät ein. Es können gefährliche Spannungen anliegen. Leitfähige Fremdobjekte können einen Kurzschluss verursachen, der einen Brand, Stromschlag oder Geräteschaden herbeiführen kann.

Symbole

Die Symbole in diesem Handbuch haben folgende Bedeutung:

Achtung – Gefahr von Verletzung und Geräteschaden. Befolgen Sie die Anweisungen.

Achtung – Heiße Oberfläche. Nicht berühren, da Verletzungsgefahr durch heiße Oberfläche besteht.

Achtung – Gefährliche Spannungen. Befolgen Sie die Anweisungen, um Stromschläge und Verletzungen zu vermeiden.

Je nach Netzschaltertyp an Ihrem Gerät kann eines der folgenden Symbole verwendet werden:

Ein – Versorgt das System mit Wechselstrom.

Aus– Unterbricht die Wechselstromzufuhr zum Gerät.

Wartezustand – Der Ein-/Standby-Netzschalter befindet sich in der Standby-Position.

Modifikationen des Geräts

Nehmen Sie keine elektrischen oder mechanischen Gerätemodifikationen vor. Sun Microsystems ist für die Einhaltung der Sicherheitsvorschriften von modifizierten Sun-Produkten nicht haftbar.

Aufstellung von Sun-Geräten

Achtung – Geräteöffnungen Ihres Sun-Produkts dürfen nicht blockiert oder abgedeckt werden. Sun-Geräte sollten niemals in der Nähe von Heizkörpern oder Heißluftklappen aufgestellt werden. Die Nichtbeachtung dieser Richtlinien kann Überhitzung verursachen und die Zuverlässigkeit Ihres Sun-Geräts beeinträchtigen.

Lautstärke

Gemäß den in DIN 45 635 Teil 1000 definierten Vorschriften beträgt die arbeitsplatzbedingte Lautstärke dieses Produkts weniger als 70 dB(A).

SELV-Konformität

Der Sicherheitsstatus der E/A-Verbindungen entspricht den SELV-Anforderungen.

Anschluss des Netzkabels

Achtung – Sun-Geräte sind für Stromversorgungssysteme mit einem geerdeten neutralen Leiter (geerdeter Rückleiter bei gleichstrombetriebenen Geräten) ausgelegt. Um die Gefahr von Stromschlägen zu vermeiden, schließen Sie das Gerät niemals an andere Stromversorgungssysteme an. Wenden Sie sich an den zuständigen Gebäudeverwalter oder an einen qualifizierten Elektriker, wenn Sie nicht sicher wissen, an welche Art von Stromversorgungssystem Ihr Gebäude angeschlossen ist.

Achtung – Nicht alle Netzkabel verfügen über die gleichen Nennwerte. Herkömmliche, im Haushalt verwendete Verlängerungskabel besitzen keinen Überlastschutz und sind daher für Computersysteme nicht geeignet. Verwenden Sie bei Ihrem Sun-Produkt keine Haushalts-Verlängerungskabel.

Die folgende Warnung gilt nur für Geräte mit Standby-Netzschalter:

Achtung – Beim Netzschalter dieses Geräts handelt es sich nur um einen Ein/Standby-Schalter. Zum völligen Abtrennen des Systems von der Stromversorgung dient hauptsächlich das Netzkabel. Stellen Sie sicher, dass das Netzkabel an eine frei zugängliche geerdete Steckdose in der Nähe des Systems angeschlossen ist. Schließen Sie das Stromkabel nicht an, wenn die Stromversorgung vom Systemchassis entfernt wurde.

Die folgende Warnung gilt nur für Geräte mit mehreren Netzkabeln:

Achtung – Bei Produkten mit mehreren Netzkabeln müssen alle Netzkabel abgetrennt werden, um das System völlig von der Stromversorgung zu trennen.

Warnung bezüglich Batterien

Achtung – Bei unsachgemäßer Handhabung oder nicht fachgerechtem Austausch der Batterien besteht Explosionsgefahr. Verwenden Sie bei Systemen mit austauschbaren Batterien ausschließlich Ersatzbatterien desselben Typs und Herstellers bzw. einen entsprechenden, vom Hersteller gemäß den Anweisungen im Service-Handbuch des Produkts empfohlenen Batterietyp. Versuchen Sie nicht, die Batterien auszubauen oder außerhalb des Systems wiederaufzuladen. Werfen Sie die Batterien nicht ins Feuer. Entsorgen Sie die Batterien entsprechend den Anweisungen des Herstellers und den vor Ort geltenden Vorschriften. CPU-Karten von Sun verfügen über eine Echtzeituhr mit integrierter Lithiumbatterie. Diese Batterie darf nur von einem qualifizierten Servicetechniker ausgewechselt werden.

Gehäuseabdeckung

Sie müssen die Abdeckung Ihres Sun-Computersystems entfernen, um Karten, Speicher oder interne Speichergeräte hinzuzufügen. Bringen Sie vor dem Einschalten des Systems die Gehäuseabdeckung wieder an.

Achtung – Nehmen Sie Sun-Geräte nicht ohne Abdeckung in Betrieb. Die Nichtbeachtung dieses Warnhinweises kann Verletzungen oder Geräteschaden zur Folge haben.

Warnungen bezüglich in Racks eingebauter Systeme

Die folgenden Warnungen gelten für Racks und in Racks eingebaute Systeme:

Achtung – Aus Sicherheitsgründen sollten sämtliche Geräte von unten nach oben in Racks eingebaut werden. Installieren Sie also zuerst die Geräte, die an der untersten Position im Rack eingebaut werden, gefolgt von den Systemen, die an nächsthöherer Stelle eingebaut werden, usw.

Achtung – Verwenden Sie beim Einbau den Kippschutz am Rack, um ein Umkippen zu vermeiden.

Achtung – Um extreme Betriebstemperaturen im Rack zu vermeiden, stellen Sie sicher, dass die Maximaltemperatur die Nennleistung der Umgebungstemperatur für das Produkt nicht überschreitet

Achtung – Um extreme Betriebstemperaturen durch verringerte Luftzirkulation zu vermeiden, sollte die für den sicheren Betrieb des Geräts erforderliche Luftzirkulation eingesetzt werden.

Hinweis zur Laser-Konformität

Sun-Produkte, die die Laser-Technologie verwenden, entsprechen den Laser-Anforderungen der Klasse 1.

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CD- und DVD-Geräte

Die folgende Warnung gilt für CD-, DVD- und andere optische Geräte:

Achtung – Die hier nicht aufgeführte Verwendung von Steuerelementen, Anpassungen oder Ausführung von Vorgängen kann eine gefährliche Strahlenbelastung verursachen.

Normativas de seguridad

Lea esta sección antes de realizar cualquier operación. En ella se explican las medidas de seguridad que debe tomar al instalar un producto de Sun Microsystems.

Medidas de seguridad

Para su protección, tome las medidas de seguridad siguientes durante la instalación del equipo:

- Siga todos los avisos e instrucciones indicados en el equipo.
- Asegúrese de que el voltaje y frecuencia de la fuente de alimentación coincidan con el voltaje y frecuencia indicados en la etiqueta de clasificación eléctrica del equipo.
- No introduzca objetos de ningún tipo por las rejillas del equipo, ya que puede quedar expuesto a voltajes peligrosos. Los objetos conductores extraños pueden producir cortocircuitos y, en consecuencia, incendios, descargas eléctricas o daños en el equipo.

Símbolos

En este documento aparecen los siguientes símbolos:

Precaución – Existe el riesgo de que se produzcan lesiones personales y daños en el equipo. Siga las instrucciones.

Precaución – Superficie caliente. Evite todo contacto. Las superficies están calientes y pueden causar lesiones personales si se tocan.

Precaución – Voltaje peligroso. Para reducir el riesgo de descargas eléctricas y lesiones personales, siga las instrucciones.

En función del tipo de interruptor de alimentación del que disponga el dispositivo, se utilizará uno de los símbolos siguientes:

Encendido – Suministra alimentación de CA al sistema.

Apagado – Corta la alimentación de CA del sistema.

Espera – El interruptor de encendido/espera está en la posición de espera.

Modificaciones en el equipo

No realice modificaciones de tipo mecánico ni eléctrico en el equipo. Sun Microsystems no se hace responsable del cumplimiento de normativas en caso de que un producto Sun se haya modificado.

Colocación de un producto Sun

Precaución – No obstruya ni tape las rejillas del producto Sun. Nunca coloque un producto Sun cerca de radiadores ni fuentes de calor. Si no sigue estas indicaciones, el producto Sun podría sobrecalentarse y la fiabilidad de su funcionamiento se vería afectada.

Nivel de ruido

De conformidad con los requisitos establecidos en el apartado 1000 de la norma DIN 45635, el nivel de ruido en el lugar de trabajo producido por este producto es menor de 70 db(A).

Cumplimiento de la normativa para instalaciones SELV

Las condiciones de seguridad de las conexiones de entrada y salida cumplen los requisitos para instalaciones SELV (del inglés *Safe Extra Low Voltage*, voltaje bajo y seguro).

Conexión del cable de alimentación

Precaución – Los productos Sun se han diseñado para funcionar con sistemas de alimentación que cuenten con un conductor neutro a tierra (con conexión a tierra de regreso para los productos con alimentación de CC). Para reducir el riesgo de descargas eléctricas, no conecte ningún producto Sun a otro tipo de sistema de alimentación. Póngase en contacto con el encargado de las instalaciones de su empresa o con un electricista cualificado en caso de que no esté seguro del tipo de alimentación del que se dispone en el edificio.

Precaución – No todos los cables de alimentación tienen la misma clasificación eléctrica. Los alargadores de uso doméstico no cuentan con protección frente a sobrecargas y no están diseñados para su utilización con sistemas informáticos. No utilice alargadores de uso doméstico con el producto Sun.

La siguiente medida solamente se aplica a aquellos dispositivos que dispongan de un interruptor de alimentación de espera:

Precaución – El interruptor de alimentación de este producto funciona solamente como un dispositivo de espera. El cable de alimentación hace las veces de dispositivo de desconexión principal del sistema. Asegúrese de que conecta el cable de alimentación a una toma de tierra situada cerca del sistema y de fácil acceso. No conecte el cable de alimentación si la unidad de alimentación no se encuentra en el bastidor del sistema.

La siguiente medida solamente se aplica a aquellos dispositivos que dispongan de varios cables de alimentación:

Precaución – En los productos que cuentan con varios cables de alimentación, debe desconectar todos los cables de alimentación para cortar por completo la alimentación eléctrica del sistema.

Advertencia sobre las baterías

Precaución – Si las baterías no se manipulan o reemplazan correctamente, se corre el riesgo de que estallen. En los sistemas que cuentan con baterías reemplazables, reemplácelas sólo con baterías del mismo fabricante y el mismo tipo, o un tipo equivalente recomendado por el fabricante, de acuerdo con las instrucciones descritas en el manual de servicio del producto. No desmonte las baterías ni intente recargarlas fuera del sistema. No intente deshacerse de las baterías echándolas al fuego. Deshágase de las baterías correctamente de acuerdo con las instrucciones del fabricante y las normas locales. Tenga en cuenta que en las placas CPU de Sun, hay una batería de litio incorporada en el reloj en tiempo real. Los usuarios no deben reemplazar este tipo de baterías.

Cubierta de la unidad del sistema

Debe extraer la cubierta de la unidad del sistema informático Sun para instalar tarjetas, memoria o dispositivos de almacenamiento internos. Vuelva a colocar la cubierta antes de encender el sistema informático.

Precaución – No ponga en funcionamiento los productos Sun que no tengan colocada la cubierta. De lo contrario, puede sufrir lesiones personales y ocasionar daños en el sistema.

Advertencia sobre el sistema en bastidor

Las advertencias siguientes se aplican a los sistemas montados en bastidor y a los propios bastidores.

Precaución – Por seguridad, siempre deben montarse los equipos de abajo arriba. A saber, primero debe instalarse el equipo que se situará en el bastidor inferior; a continuación, el que se situará en el siguiente nivel, etc.

Precaución – Para evitar que el bastidor se vuelque durante la instalación del equipo, debe extenderse la barra antivolcado del bastidor.

Precaución – Para evitar que se alcance una temperatura de funcionamiento extrema en el bastidor, asegúrese de que la temperatura máxima no sea superior a la temperatura ambiente establecida como adecuada para el producto.

Precaución – Para evitar que se alcance una temperatura de funcionamiento extrema debido a una circulación de aire reducida, debe considerarse la magnitud de la circulación de aire requerida para que el equipo funcione de forma segura.

Aviso de cumplimiento de la normativa para la utilización de láser

Los productos Sun que utilizan tecnología láser cumplen los requisitos establecidos para los productos láser de clase 1.

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Dispositivos de CD y DVD

La siguiente medida se aplica a los dispositivos de CD y DVD, así como a otros dispositivos ópticos:

Precaución – La utilización de controles, ajustes o procedimientos distintos a los aquí especificados puede dar lugar a niveles de radiación peligrosos.

Nordic Lithium Battery Cautions

Norge

Advarsel – Litiumbatteri — Eksplosjonsfare. Ved utskifting benyttes kun batteri som anbefalt av apparatfabrikanten. Brukt batteri returneres apparatleverandøren.

Sverige

Varning – Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.

Danmark

Advarsel! – Litiumbatteri — Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.

Suomi

Varoitus – Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

Regulatory Compliance Statements

Your Sun product is marked to indicate its compliance class:

- Federal Communications Commission (FCC) — USA
- Industry Canada Equipment Standard for Digital Equipment (ICES-003) — Canada
- Voluntary Control Council for Interference (VCCI) — Japan
- Bureau of Standards Metrology and Inspection (BSMI) — Taiwan

Please read the appropriate section that corresponds to the marking on your Sun product before attempting to install the product.fc

FCC Class A Notice

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy, and if it is not installed and used in accordance with the instruction manual, it may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

Modifications: Any modifications made to this device that are not approved by Sun Microsystems, Inc. may void the authority granted to the user by the FCC to operate this equipment.

FCC Class B Notice

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio / television technician for help.

Modifications: Any modifications made to this device that are not approved by Sun Microsystems, Inc. may void the authority granted to the user by the FCC to operate this equipment.

ICES-003 Class A Notice - Avis NMB-003, Classe A

This Class A digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de la classe A est conforme à la norme NMB-003 du Canada.

ICES-003 Class B Notice - Avis NMB-003, Classe B

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada.

VCCI 基準について

クラス A VCCI 基準について

クラス A VCCI の表示があるワークステーションおよびオプション製品は、クラス A 情報技術装置です。これらの製品には、下記の項目が該当します。

この装置は、情報処理装置等電波障害自主規制協議会 (VCCI) の基準に基づくクラス A 情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。

クラス B VCCI 基準について

クラス B VCCI の表示  があるワークステーションおよびオプション製品は、クラス B 情報技術装置です。これらの製品には、下記の項目が該当します。

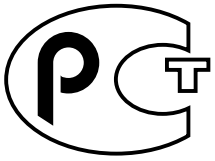
この装置は、情報処理装置等電波障害自主規制協議会 (VCCI) の基準に基づくクラス B 情報技術装置です。この装置は、家庭環境で使用することを目的としていますが、この装置がラジオやテレビジョン受信機に近接して使用されると、受信障害を引き起こすことがあります。取扱説明書に従って正しい取り扱いをしてください。

BSMI Class A Notice

The following statement is applicable to products shipped to Taiwan and marked as Class A on the product compliance label.

警告使用者：
這是甲類的資訊產品，在居住的環境中使用
時，可能會造成射頻 干擾，在這種情況下，
使用者 會被要求採取某些適當的對策。

GOST-R Certification Mark



Shielded Cables

English

Hardwire connections between the workstations and peripherals must be made using shielded cables to comply with radio frequency emission limits. Hardwire Network connections can be made using unshielded twisted-pair (UTP) cables.

French

Les connexions par raccordements fixes entre les stations de travail et les périphériques doivent être effectuées à l'aide de câbles blindés, conformément aux limites d'émission de la fréquence radio. Les connexions au réseau par raccordements fixes peuvent être effectuées à l'aide de câbles à paires torsadées non blindées.

German

Kabelverbindungen zwischen Workstations und Peripheriegeräten müssen mithilfe von abgeschirmten Kabeln hergestellt werden, um den Grenzwerten für die Hochfrequenzabstrahlung zu entsprechen. Die Verkabelung für Netzwerkverbindungen kann mithilfe von ungeschirmten Twisted-Pair-Kabeln (UTP) eingerichtet werden.

Spanish

En las conexiones de cableado entre las estaciones de trabajo y los periféricos deben utilizarse cables blindados para cumplir con los límites de emisiones de radiofrecuencia. En las conexiones de cableado de red pueden utilizarse cables de par trenzado no blindados.

Declaration of Conformity

Compliance Model Number: SBD1F
Product Family Name: Netra CP2300 Telecom Blade Server

EMC

USA—FCC Class A

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This equipment may not cause harmful interference.
2. This equipment must accept any interference that may cause undesired operation.

European Union

This equipment complies with the following requirements of the EMC Directive 89/336/EEC:

As Telecommunication Network Equipment (TNE) in both Telecom Centers and Other Than Telecom Centers per (as applicable):

EN300-386 V.1.3.1 (09-2001) Required Limits:

EN55022/CISPR22	Class A
EN61000-3-2	Pass
EN61000-3-3	Pass
EN61000-4-2	6 kV (Direct), 8 kV (Air)
EN61000-4-3	3 V/m 80-1000MHz, 10 V/m 800-960 MHz, and 1400-2000 MHz
EN61000-4-4	1 kV AC and DC Power Lines, 0.5 kV Signal Lines
EN61000-4-5	2 kV AC Line-Gnd, 1 kV AC Line-Line and Outdoor Signal Lines, 0.5 kV Indoor signal Lines > 10m
EN61000-4-6	3 V
EN61000-4-11	Pass

As Information Technology Equipment (ITE) Class A per (as applicable):

EN55022:1998/CISPR22:1997	Class A
EN55024:1998 Required Limits:	
EN61000-4-2	4 kV (Direct), 8 kV (Air)
EN61000-4-3	3 V/m
EN61000-4-4	1 kV AC Power Lines, 0.5 kV Signal and DC Power Lines
EN61000-4-5	1 kV AC Line-Line and Outdoor Signal Lines, 2 kV AC Line-Gnd, 0.5 kV DC Power Lines
EN61000-4-6	3 V
EN61000-4-8	1 A/m
EN61000-4-11	Pass
EN61000-3-2:1995 + A1, A2, A14	Pass
EN61000-3-3:1995	Pass

Safety

This equipment complies with the following requirements of the Low Voltage Directive 73/23/EEC:

EC Type Examination Certificates:

EN60950:2000, 3rd Edition	TÜV Rheinland Certificate No.
IEC 60950:1999, 3rd Edition	CB Scheme Certificate No. US/7056/UL
Evaluated to all CB Countries	
UL 60950, 3rd Edition, CSA C22.2 No. 60950-00	File: E138989-A11-UL-1

Supplementary Information: This product was tested and complies with all the requirements for the CE Mark.

/S/

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Declaration of Conformity

Compliance Model Number: SBD1R
Product Family Name: Netra CP2300 Telecom Blade Server Rear Transition Card (XCP-2300TRN)

EMC

USA—FCC Class A

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This equipment may not cause harmful interference.
2. This equipment must accept any interference that may cause undesired operation.

European Union

This equipment complies with the following requirements of the EMC Directive 89/336/EEC:

As Telecommunication Network Equipment (TNE) in both Telecom Centers and Other Than Telecom Centers per (as applicable):

EN300-386 V.1.3.1 (09-2001) Required Limits:

EN55022/CISPR22	Class A
EN61000-3-2	Pass
EN61000-3-3	Pass
EN61000-4-2	6 kV (Direct), 8 kV (Air)
EN61000-4-3	3 V/m 80-1000MHz, 10 V/m 800-960 MHz, and 1400-2000 MHz
EN61000-4-4	1 kV AC and DC Power Lines, 0.5 kV Signal Lines
EN61000-4-5	2 kV AC Line-Gnd, 1 kV AC Line-Line and Outdoor Signal Lines, 0.5 kV Indoor signal Lines > 10m
EN61000-4-6	3 V
EN61000-4-11	Pass

As Information Technology Equipment (ITE) Class A per (as applicable):

EN55022:1998/CISPR22:1997	Class A

EN55024:1998 Required Limits:

EN61000-4-2	4 kV (Direct), 8 kV (Air)
EN61000-4-3	3 V/m
EN61000-4-4	1 kV AC Power Lines, 0.5 kV Signal and DC Power Lines
EN61000-4-5	1 kV AC Line-Line and Outdoor Signal Lines, 2 kV AC Line-Gnd, 0.5 kV DC Power Lines
EN61000-4-6	3 V
EN61000-4-8	1 A/m
EN61000-4-11	Pass
EN61000-3-2:1995 + A1, A2, A14	Pass
EN61000-3-3:1995	Pass

Safety

This equipment complies with the following requirements of the Low Voltage Directive 73/23/EEC:

EC Type Examination Certificates:

EN60950:2000, 3rd Edition	TÜV Rheinland Certificate No.
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Evaluated to all CB Countries	
UL 60950, 3rd Edition, CSA C22.2 No. 60950-00	File: E138989-A11-UL-1

Supplementary Information: This product was tested and complies with all the requirements for the CE Mark.

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Preface

The *Netra CP2300 cPSB Board Installation and Technical Reference Manual* describes the hardware specifications, function and physical properties of the Netra™ CP2300 CompactPCI packet switched backplane (cPSB) board.

The *Netra CP2300 cPSB Board Installation and Technical Reference Manual* is written for system integration engineers, field applications and service engineers, and others involved in the integration of these boards into systems.

How This Book Is Organized

Chapter 1 provides an overview of the Netra CP2300 board.

Chapter 2 provides instructions on hardware installation.

Chapter 3 provides instructions on the software configuration.

Chapter 4 provides information on the Netra CP2300 board OpenBoot™ firmware and Power-on Self Test (POST).

Chapter 5 provides a description of the various hardware blocks on the Netra CP2300 board.

Appendix A provides information on the Netra CP2300 board specifications.

Appendix B provides pinouts of the Netra CP2300 board connectors.

Appendix C describes how to access the Solaris™ Sun™ FRU ID information for a Netra CP2300 board.

Appendix D provides a comprehensive list of references for the Netra CP2300 board.

The Glossary lists definitions of many of the special terms used in this publication.

Related Documentation

For additional information about the Netra CP2300 cPSB board or the Netra CP2300 cPSB transition card, refer to the following documents:

- *Netra CP2300 cPSB Board Installation and Technical Reference Manual* (816-7186-*xx*)
- *Netra CP2300 cPSB Board Product Note* (816-7185-*xx*)
- *Netra CP2300 cPSB Board Release Notes* (817-1741-*xx*)
- *Netra CP2300 cPSB Transition Card Installation and Technical Reference Manual* (816-7188-*xx*)
- *Netra CP2300 cPSB Transition Card Product Note* (816-7187-*xx*)
- *Netra CP2300 cPSB Board Programming Guide* (817-1331-*xx*)
- *Important Safety Information for Sun Hardware Systems* (816-7190-*xx*)

Appendix D lists additional related documentation.

Accessing Sun Documentation

You can view, print, or purchase a broad selection of Sun documentation, including localized versions, at:

`http://www.sun.com/documentation`

Typographic Conventions

Typeface*	Meaning	Examples
`AaBbCc123`	The names of commands, files, and directories; on-screen computer output	Edit your `.login` file. Use `ls -a` to list all files. `% You have mail.`
`AaBbCc123`	What you type, when contrasted with on-screen computer output	`% su` `Password:`
AaBbCc123	Book titles, new words or terms, words to be emphasized. Replace command-line variables with real names or values.	Read Chapter 6 in the *User's Guide*. These are called *class* options. You *must* be superuser to do this. To delete a file, type `rm` *filename*.

* The settings on your browser might differ from these settings.

Shell Prompts

Shell	Prompt
C shell	*machine-name*%
C shell superuser	*machine-name*#
Bourne shell and Korn shell	$
Bourne shell and Korn shell superuser	#

Using UNIX Commands

This document might not contain information on basic UNIX® commands and procedures such as shutting down the system, booting the system, and configuring devices.

See one or more of the following for this information:

- *Solaris Handbook for Sun Peripherals*
- AnswerBook2™ online documentation for the Solaris™ operating environment
- Other software documentation that you received with your system

Contacting Sun Technical Support

If you have technical questions about this product that are not answered in this document, go to:

`http://www.sun.com/service/contacting`

Sun Welcomes Your Comments

Sun is interested in improving its documentation and welcomes your comments and suggestions. You can submit your comments by going to:

`http://www.sun.com/hwdocs/feedback`

Please include the title and part number of your document with your feedback:

Netra CP2300 cPSB Board Installation and Technical Reference Manual, part number 816-7186-12

CHAPTER 1

Overview of the Netra CP2300 cPSB Board

The Netra CP2300 cPSB board is a crucial building block that network equipment providers (NEPs) and carriers can use when scaling and improving the availability of carrier-grade systems. Based on industry standards, the Netra CP2300 board provides high performance and is powered by a 650 MHz UltraSPARC IIi processor.

The Netra CP2300 board enables customers to mix and match third-party PCI mezzanine cards (PMCs), making it easier for them to tailor solutions to their specific application needs. The Netra CP2300 board provides PCI Industrial Computers Manufacturers' Group (PICMG) CompactPCI Packet Switched Backplane compliance (for details, see TABLE 1-1) and is NEBS Level 3 certified to meet the requirements of the communications and service provider environments.

This chapter contains the following sections:

1.1 Features of the Netra CP2300 cPSB Board

The Netra CP2300 board is a cPSB single-board computer designed for high-performance embedded, compute density applications. The Netra CP2300 board has System Management Controller (SMC) capability that supports hot-swap operations, system management, and environmental monitoring. Powered by a 650 MHz UltraSPARC IIi processor, and including two the PMC slots, the Netra CP2300 board is an ideal platform for NEPs to use for a wide variety of Solaris applications.

FIGURE 1-1 displays an illustration of a typical Netra CP2300 board, and TABLE 1-1 lists a summary of features of the board.

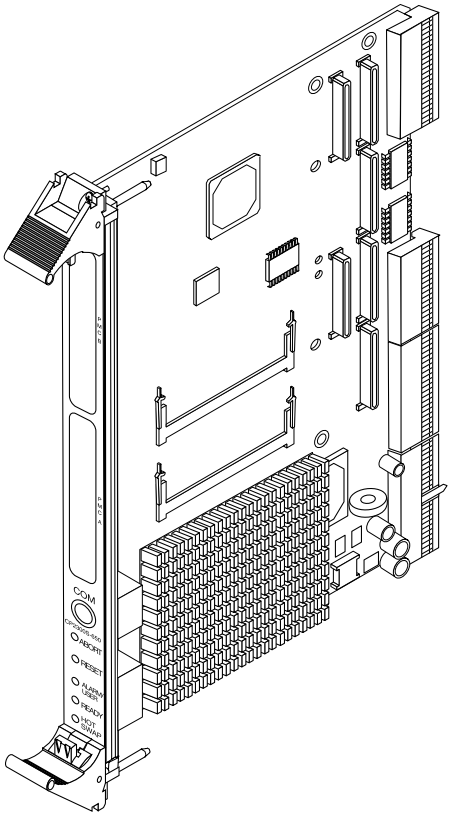

FIGURE 1-1 Typical Netra CP2300 cPSB Board

TABLE 1-1 Feature Summary

Feature	Description
CPU	UltraSPARC IIi 650 MHz processor with internal L2 cache (2:2 mode, 512 Kbyte, 4-way set association)
Memory	512 MB on-board memory, with two PC133 compliant DRAM EEC SO-DIMM slots available for additional memory expansion
Power requirement	Estimated at 22W (typical) and 26W (peak maximum) at 650 MHz, and 30W (peak maximum) with two 512 MB SO-DIMMs installed (The power requirements exclude PMC, SO-DIMM memory, and rear transition card power.)
PICMG and PCI compliance	• PICMG 2.0 R3.0 CompactPCI bus specification for 33MHz PCI speed • PICMG 2.1 R2.0 Hot-Swap Specification • PICMG 2.10 R1.0 Keying of cPCI boards and backplanes • PICMG 2.15 R1.0 PCI Telecom Mezzanine/Carrier Cards (PTMC) support • PICMG 2.16 R1.0 CompactPCI Packet Switching Backplane • PICMG 2.3 R1.0 PMC on CompactPCI Tables 1 and 3 • PICMG 2.9 R1.0 System Management Specification • PMC Specification P1386 Draft 2.4 • CMC P1386 Draft 2.4 Standard for CMC
Node Board support	The board functions as a cPSB node board with the Solaris software package
IPMI system management	Uses IPMI communications with Baseboard Management Controller (BMC); performs environmental monitoring on local board interface for example temperature sense, FRU ID, and control
Hot-swap support	Basic, Full, and High-Availability (HA) hot-swap support
Operating system	Solaris 8 operating environment, Release 2/02, and subsequent compatible versions
Front I/O and connectors	• Two PMC slots • One serial port (can only be used if rear serial port COM A is not used)
Connectors on rear transition card (optional)	• Two 10/100 Ethernet ports (switch selectable and mutually exclusive with cPSB networks) • Two serial ports • One USB port • Two PCI Interface Module (PIM) slots • 40-pin EIDE connector on board (not on panel) (EIDE connector is switch selectable and mutually exclusive with PIM A I/O 1-29.)

TABLE 1-1 Feature Summary *(Continued)*

Feature	Description
PMC I/O	Provision for adding up to two independent hardware vendor (IHV) supplied PMC expansion ports on front panel.
Backplane PMC I/O	One USB port; also provision for adding two IHV-supplied PIM I/O ports when used with transition card
Watchdog timer	Two-level watchdog timer
NVRAM	8 Kbyte non-volatile I^2C SEEPROM to save OpenBoot PROM configuration. TOD has no battery backup as battery backup is not needed.
System flash	1 Mbyte on board
User flash	7 Mbyte on board
Building compliance	NEBS Level 3
Flash update	Supported from downloaded file

Note – For EMI compliance of front access ports, use shielded cables on all I/O ports. The shields for all shielded cables must be terminated on both ends.

1.2 Netra CP2300 Board System Configurations

The Netra CP2300 boards can be mounted in various enclosures, such as shown in FIGURE 1-2. The boards can be deployed in various electrical configurations to suit each end-user requirement. For example, the board can be configured to boot from a network as a diskless client with either a cPSB or rear transition card network connection. Alternatively, industry-standard PMC and PIM hardware from independent hardware vendors (IHVs) can be installed to provide local disk I/O, which may optionally be used as a boot path. The installation procedure is independent of the type of enclosure, whether a floor-mounting rack or a bench-top cabinet is used. The Netra CP2300 board has fixed on-board memory and connectors for additional memory.

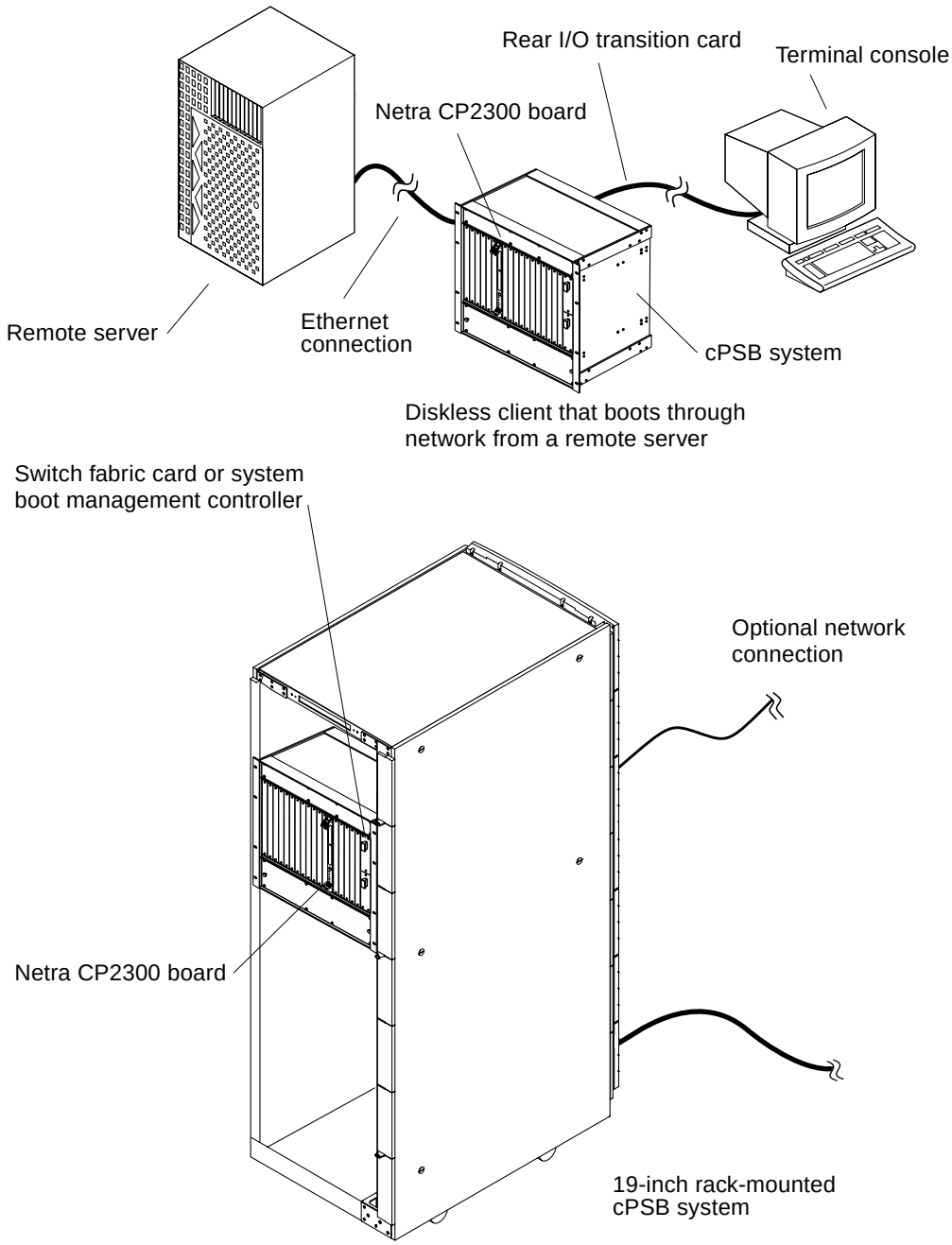

FIGURE 1-2 Netra CP2300 cPSB Board Mounting Configuration Examples

1.2.1 PMC and PIM Modules

The Netra CP2300 board has one serial port on the front panel. The IHV-built PMC modules provide additional I/O to the front panels. PMC modules decode their custom I/O from the Netra board's on-board PCI bus A signals. A transition card can also be fitted with IHV PCI Interface Modules (PIM) to bring I/O channels to the rear of the unit. See Section 5.4.2, "PMC and PIM Interface" on page 5-12 for further information.

1.2.2 Rear Transition Card

The optional Netra CP2300 cPSB transition card (Sun part number, XCP2300-TRN) installs into the rear of the cPSB enclosure, opposite the Netra CP2300 board (see FIGURE 1-4). The transition card connects with the host CompactPCI connectors through the backplane pins and carries two serial ports and a USB port out to its rear-panel flange. The transition card contains a 40-pin EIDE connector that is switch selectable and mutually exclusive with the PIM A connector I/O pins 1-29. The transition card also provides two switch-selectable RJ-45 10/100 Ethernet connectors, which are mutually exclusive with cPSB network interfaces. The Netra CP2300 board SW3 DIP switch controls the access to these Ethernet ports (see Section B.5, "DIP Switch Settings" on page B-20 for more information).

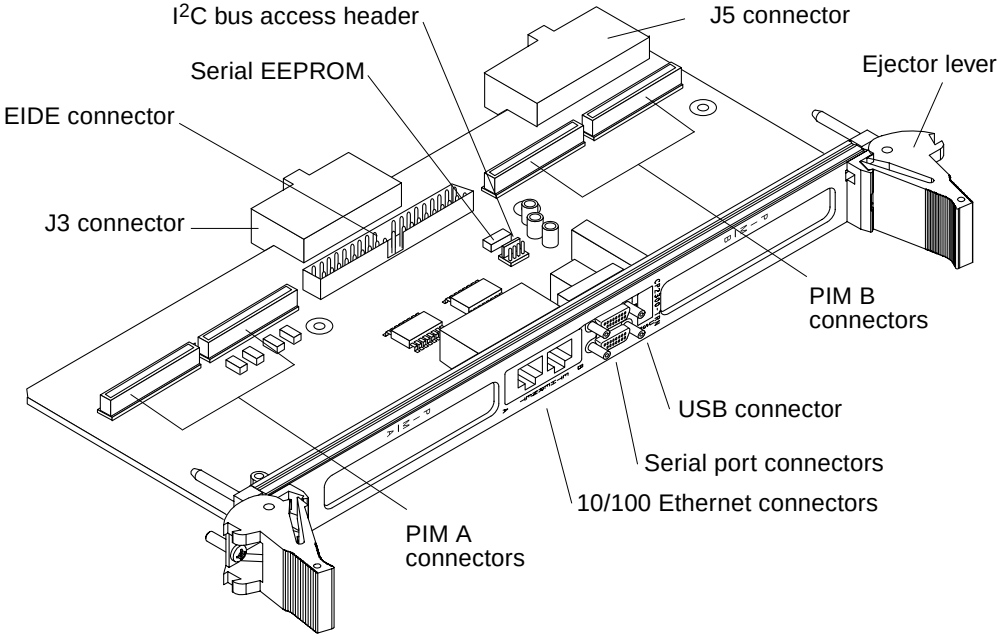

FIGURE 1-3 Netra CP2300 cPSB Board Rear Transition Card

FIGURE 1-4 show the physical relationship between the board, transition card, and the backplane in a typical cPSB system.

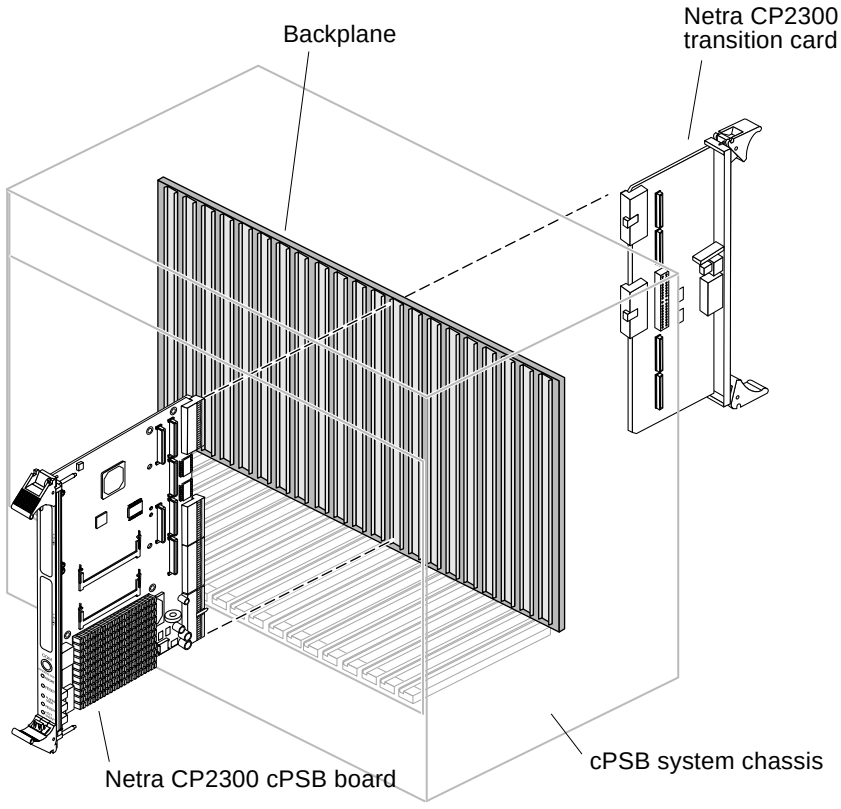

FIGURE 1-4 Typical cPSB System Chassis Illustrating the Netra CP2300 Board and the Netra CP2300 Transition Card

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Note – When the transition card is used with the Netra CP2300 board, shielded cables are required for serial and USB I/O ports, and unshielded cables can be used on Ethernet ports in order to satisfy EMI compliance standards. The shields for all shielded cables must be terminated on both ends.

The transition card can also be fitted with IHV PIM modules which are configured to bring I/O channels to the unit rear panel. A PIM hardware kit includes a card for the PMC slot and a card for the PIM slot on the transition card. A PIM is a rear-panel extension added to a PMC module. When the PIM I/O is configured, the front PMC I/O output is not accessible.

The customer can order the Netra CP2300 transition card, build a custom card, or buy from an Independent Hardware Vendor (IHV). A minimal set of I/O must provide for a boot path for the host board and for a path for console I/O to deliver commands and to read board and system status.

Possible boot and console configurations are described in TABLE 1-2. Sun Microsystems provides the Netra CP2300 board and a compatible Netra CP2300 transition card. This transition card provides two 10/100 Ethernet RJ45 ports from the host to the rear of the system, which can optionally be used to accomplish a network boot as a diskless client. The other configurations require IHV hardware.

TABLE 1-2 Netra CP2300 Board I/O Configurations

I/O	Hardware Required	Description
Ethernet	Netra CP2300 transition card—supplied as an option for rear access	Default boot path uses cPSB Ethernet port; board runs in diskless client configuration.
SCSI	Netra CP2300 transition card; PMC SCSI I/O	May be used for local boot; requires optional transition card with PMC SCSI I/O.
Serial data	Netra CP2300 board	Serial port A on front panel provides the path of the default console I/O.
	Netra CP2300 transition card	When optional transition card is installed, the card's serial port A will become the path of the default console I/O (see FIGURE 1-3 for location).
USB	Netra CP2300 transition card	Can be used for keyboard I/O.

1.3 Hot-Swap Support

This section briefly discusses the hot-swap support on the Netra CP2300 board.

See Appendix D for a reference to the PICMG *CompactPCI Hot Swap Specification* which provides a detailed description of this subject. In general, the hot-swap process includes the orderly connection of the hardware and software.

This process uses hardware connection control to connect the hardware in an orderly sequence. This process includes the use of backplane pins of different lengths to accomplish signal sequencing to protect the hardware and avoid corrupting the backplane bus.

There are three models of hot swap described in the PICMG *CompactPCI Hot Swap Specification*: basic hot-swap, full hot-swap, and high-availability (HA) hot-swap.

TABLE 1-3 lists the hot-swap support details when a Netra CP2300 board functions as a node board.

TABLE 1-3 Netra CP2300 Board Hot-Swap Support

Netra CP2300 Role	Basic Hot-Swap	Full Hot-Swap	HA Hot-Swap*
Node board role	Yes	Yes	Yes

* When a board is full hot-swap capable, it implies that the board will also be fully hot-swappable in an HA system.

1.4 System Requirements

1.4.1 Hardware Requirements

Sun provides these items to customer order:

- Netra CP2300 cPSB board:
  - CP2300-650-512MB
  - CP2300-650-512MBLP (with low-profile memory connectors)
- Netra CP2300 cPSB transition card: XCP2300-TRN

  The transition card enables rear system I/O access to the network, to a boot device, and to a console terminal (shown in FIGURE 1-3).

  This transition card is optional and must be ordered separately from the Netra CP2300 board. See the *Netra CP2300 cPSB Transition Card Installation and Technical Reference Manual* (816-7188-*xx*) for complete details about the transition card.

You must acquire the following components if needed:

- Serial terminal or terminal emulation for console output
- Cables for terminal and network connection

  See Section B.3, “Front Panel Serial Connector” on page B-11 and *Netra CP2300 cPSB Transition Card Installation and Technical Reference Manual* (816-7188-*xx*) for descriptions of I/O connections.

- PIM and PMC hardware

TABLE 1-4 cPSB System and Other Minimum Requirements

Requirements	Netra CP2300 as Node Board
cPSB system enclosure for 6U boards (includes chassis, backplane, power supply*)†	Yes
Console output device/serial terminal	Yes
Boot device (such as hard drive or network)	Yes
Peripheral device for network access	Yes
System management controller	Yes

* See Appendix A to ensure that your system enclosure meets the power supply and cooling requirement specifications.

† See FIGURE 1-4 for a typical arrangement.

1.4.2 Software Requirements

The Solaris 8 2/02 operating environment, or subsequent compatible versions, may be used with the Netra CP2300 cPSB board. Refer to the *Netra CP2300 cPSB Board Release Notes* (817-1741-*xx*) for more Solaris operating environment information, including a list of the required software patches. You can view and download the latest version of this manual at the following web site:

`http://www.sun.com/products-n-solutions/hardware/docs/CPU_Boards/`

1.5 Technical Support and Warranty

Should you have any technical questions or support issues that are not addressed in the Netra CP2300 documentation set or on the Web site contact your local Sun Services representative. This hardware carries a 1-year return-to-depot warranty. For customers in the US or Canada, please call 1-800-USA-4SUN (1-800-872-4786). For customers in the rest of the world, find the World Wide Solution Center nearest you by visiting our web site:

`http://www.sun.com/service/contacting/solution.html`

When you call Sun Services, be sure to indicate that the Netra CP2300 was purchased separately and is not associated with a system. Please have the board identification information ready. For proper identification of the board be prepared to give the representative the board part number, serial number, and date code (see FIGURE 1-5).

1.5.1 Board Part Number, Serial Number, and Revision Number Identification

The Netra CP2300 board part number, serial number, and version can be found on stickers located on the card (see FIGURE 1-5). For proper identification of the board, please see the list below along with FIGURE 1-5.

The Sun barcode label provides the following information (see FIGURE 1-5):

- Board part number (for example, 3753129) which is the first seven digits on the barcode label.
- Board serial number (for example, 000016) which is the next six digits on the barcode label.

The Dash / Revision / Date Code label provides the following information (see FIGURE 1-5):

- Product dash number (for example, -01)
- Revision number (for example REV: 01)
- Board date code (for example, 3702, which represents the thirty-seventh week of year 2002)

The MAC address label contains the MAC address for the board in printed and barcode form. See Section 2.4.4, “Replacing the Serial EEPROM” on page 2-14 for information on installation and removal of the MAC address label.

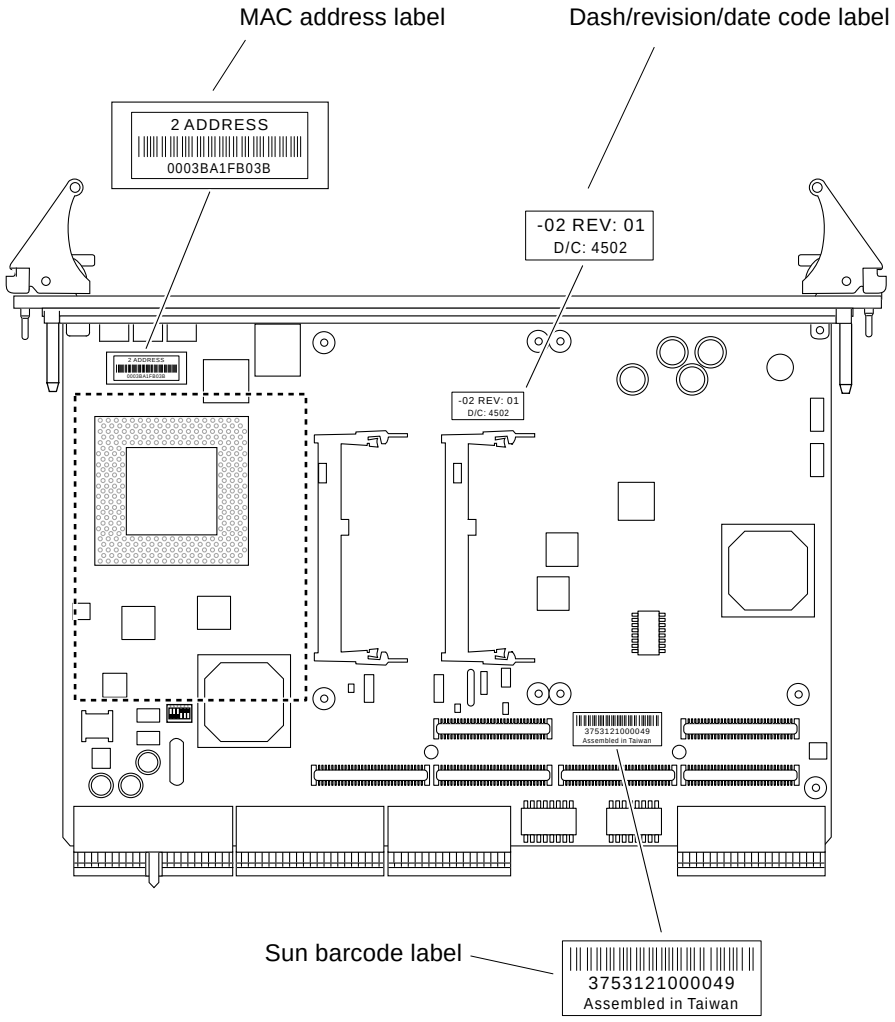

FIGURE 1-5 Typical Netra CP2300 cPSB Board Barcode Labelling

Note – You might find the labels shown in FIGURE 1-5 on other locations on your board. Also, your particular board configuration may appear different than the illustration above.

CHAPTER 2

Hardware Installation

This chapter describes the Netra CP2300 board hardware installation procedures, and contains the following sections:

2.1 Equipment and Operator Safety

Refer to the *Important Safety Information for Sun Hardware Systems* (816-7190-*xx*) for general safety information.

Read these safety statements specific to the Netra CP2300 board carefully before you install or remove any part of the system.

Caution – Depending on the particular chassis design, operations with open equipment enclosures can expose the installer to hazardous voltages with a consequent danger of electric shock. Ensure that line power to the equipment is disconnected during operations that make high voltage conductors accessible.

The installer must be familiar with commonly-accepted procedures for integrating electronic systems and with the general practice of Sun systems integration and administration. Although parts of these systems are designed for hot-swap

operation, other components must not be subjected to such stresses. Work with power connected to a chassis only when necessary and follow these installation procedures to avoid equipment damage.

This equipment is sensitive to damage from electrostatic discharge (ESD) from clothing and other materials. Use the following antistatic measures during an installation.

- If possible, disconnect line power from the equipment chassis when servicing a system or installing a hardware upgrade. If the chassis cannot be placed upon a grounded antistatic mat, connect a grounding strap between the facility electrical input ground (usually connected to the equipment chassis) and facility electrical service ground.
- Use an antistatic wrist strap when:
  - Removing a board from its antistatic bag
  - Connecting or disconnecting boards or peripherals

  The other end of the strap lead should be connected to one of the following:

  - A ground mat
  - Grounded chassis metalwork
  - A facility electrical service ground
- Keep boards in the antistatic bags until they are needed.
- Place circuit boards that are out of their antistatic bags on an antistatic mat if one is available. The mat must be grounded to a facility electrical service ground. Do not place boards on top of an antistatic bag unless the outside of the bag also has antistatic protective properties.
- Remove a board from its antistatic bag only when wearing a properly-connected ground strap.

2.2 Materials and Tools Required

This section provides information on the materials and tools required to perform installation. The minimum tools required to perform installation are:

- Straight blade screwdriver, 1/4 inch
- Phillips screwdrivers, No. 1, No. 2
- Antistatic wrist strap
- Needle nose pliers
- Needle, pick, scribe tool, or small screwdriver to set the DIP switches
- Terminal

Refer to Section 1.4.1, “Hardware Requirements” on page 1-10 for information on hardware requirements.

2.3 Preparing for the Installation

Read the following subsections before starting to install these boards. In addition, do the following:

1. Become familiar with the contents of the referenced documentation.
2. Verify that all listed hardware and software is available (see Section 1.4, “System Requirements” on page 1-10).
3. Check power, thermal, environmental and space requirements (see Section 2.3.1, “Checking Power, Thermal, Environmental, and Space Requirements” on page 2-4).
4. Verify that local area networking (LAN) preparations are completed (see Section 2.3.2, “Determining Local Network IP Addresses and Hostnames” on page 2-4).
5. Ensure that the hostnames and their network IP addresses are allocated and registered at the site.

2.3.1 Checking Power, Thermal, Environmental, and Space Requirements

Ensure that:

- Your enclosure specifications support the sum of the specified maximum board power loads. See Section A.6, “Power Requirements” on page A-7 for board power specifications.
- Facility power loading specifications can support the rack or enclosure requirements.
- Your enclosure specifications support the cooling airflow requirements. See Section A.8, “Environmental Specifications” on page A-9.
- The Netra CP2300 board fits a standard CompactPCI packet switched backplane (cPSB) chassis. If your installation requirements are different, contact your field application engineer.

2.3.2 Determining Local Network IP Addresses and Hostnames

Collect the following information to connect hosts to the local area network (LAN). Ask your network administrator for help, if necessary. This information is not needed for a standalone installation. You can use TABLE 2-1 to record this information.

TABLE 2-1 Your Local Network Information

Information Needed	Your Information
IP addresses* and hostname for each Netra CP2300 client	
Domain name	
Type of name service and corresponding name server names and IP addresses—for example DNS and NIS (or NIS+)	
Subnet mask	
Gateway router IP address	
NFS server names and IP addresses	
Web server URL	

* Local IP addresses are not needed if they are assigned by a network DHCP server

You may need the MAC (Ethernet) addresses of the local hosts to make nameserver database entries. The MAC address can be seen in the console output while booting to the ok prompt. It can also be derived from the Host ID seen on the barcode label of the I^2C EEPROM (see Section 1.5.1, “Board Part Number, Serial Number, and Revision Number Identification” on page 1-12).

2.3.3 Installation Procedure Summary

The steps in this section summarize the Netra CP2300 board installation at a high level. Make sure to read the details in Section 2.4, “Configuring the Board Hardware” on page 2-6 through Chapter 3 before installing the board.

The procedure to setup and configure a Netra CP2300 in a system includes the following steps:

1. Configure the board’s physical hardware. For example, install memory and PMC cards, replace the serial EEPROM, and set switches if necessary.
2. Configure the transition card with PIMs, switch settings, or connector attachments, as necessary.
3. Physically install the transition card (as necessary), host, and any peripheral boards into the chassis.
4. Connect the node(s) to a local network. Alternatively, the board can be run as a standalone system without a network connection.
5. Install the operating system.

2.4 Configuring the Board Hardware

This section lists hardware installation and settings that may or may not apply for your board configuration. Read and perform the procedures, as necessary, before installing the Netra CP2300 board into the chassis.

2.4.1 Installing SO-DIMM Memory Modules

In addition to the 512 MByte on-board memory, the Netra CP2300 board can accommodate two industry standard PC133 memory standard small outline dual in-line memory modules (SO-DIMMs). You can install one SO-DIMM into each socket.

Note – If you are installing only one SO-DIMM memory module to the Netra CP2300 board, you must install the module in the memory connector next to the heat sink. This connector is labeled J1 on the board, see FIGURE 2-1 for the connector's location.

The Netra CP2300 board supports SO-DIMM memory modules that have the following characteristics:

- 144-pin error-correction code (ECC) SO-DIMMs that conform to the JEDEC 21-C Standard
- PC133-compliant SDRAM
- Column access strobe (CAS) Latency 2 (CL2)
- Serial presence detect (SPD) support required
- Unregistered and Unbuffered

Note – While the JEDEC specification defines SO-DIMMs with variable heights, the Netra CP2300 board can only accommodate SO-DIMMS with heights of 1.25 inches (31.75 mm) or less.

For additional information, see Section A.4, "Memory Configuration Specifications" on page A-4.

Caution – The regular, non-low profile SO-DIMM memory connectors on the CP2300-650-512MB board configuration may interfere with PMC cards installed in PMC slot A, as these tall connectors do not meet the PMC clearance specification (they are 0.5 mm out of clearance). For PMC slot clearance information, see Section A.5.1, “PMC Specification Notes” on page A-6.

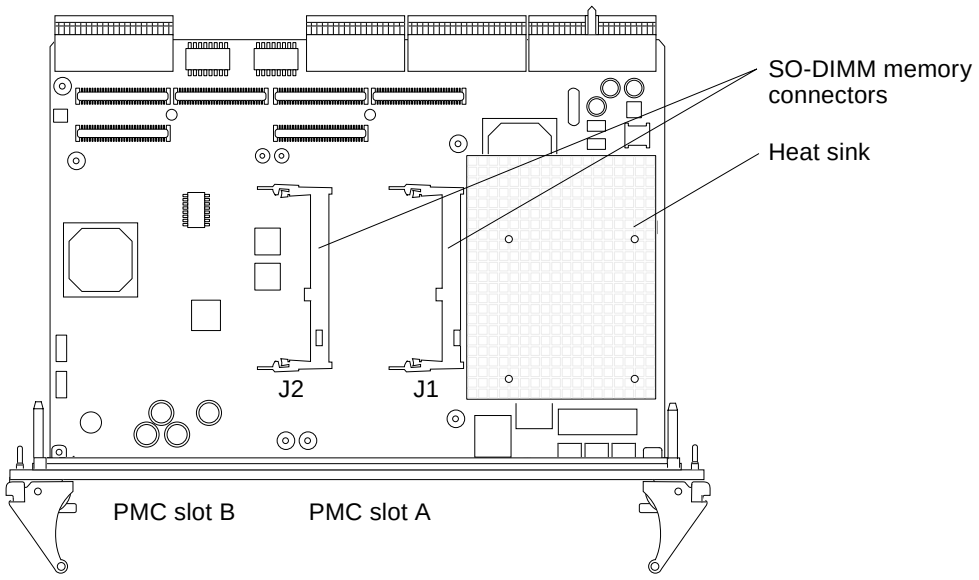

FIGURE 2-1 Location of SO-DIMM Memory and PMC Slots

2.4.1.1 To Install a SO-DIMM Memory Module

The procedure below provides a general guide for installing additional memory. However, for directions on the installation process of the memory SO-DIMMs on the Netra CP2300 board, refer to the documentation that shipped with the memory module.

Caution – Do not remove the SO-DIMM from its antistatic container until you are ready to install it on the card. Handle the module only by its edges. Do not touch module components or metal parts. Always wear a grounded antistatic wrist strap when handling modules.

1. **Locate the SO-DIMM connectors on the Netra CP2300 board.**

   Select the connector(s) where you will install the memory module (see FIGURE 2-1). If you need to replace an existing memory module with a new module, see Section 2.4.1.2, “To Remove a SO-DIMM Memory Module” on page 2-9 for instructions on removing the SO-DIMM module.

Note – If you are installing only one SO-DIMM memory module to the Netra CP2300 board, you must install the module in the memory connector next to the heat sink. This connector is labeled J1 on the board, see FIGURE 2-1 for the connector’s location.

---

2. **Remove the SO-DIMM from its protective packaging, holding the module only by the edges.**

3. **Holding the SO-DIMM at approximately a 20-degree angle to the board, insert the bottom edge of the SO-DIMM into the bottom of the slot’s hinge-style connector (see** FIGURE 2-2**).**

   The socket and module are both keyed, which means the module can be installed one way only. With even pressure, push simultaneously on both upper corners of the SO-DIMM until its bottom edge (the edge with the gold fingers) is firmly seated in the connector.

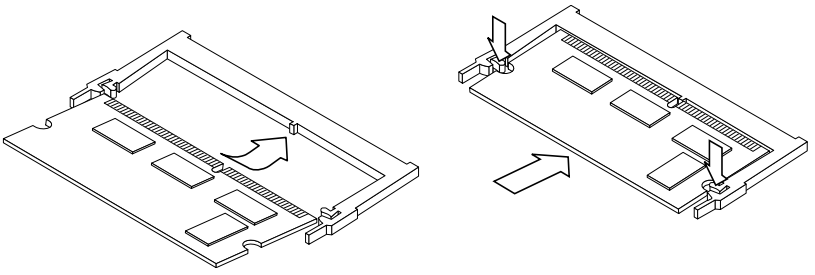

FIGURE 2-2 Installing SO-DIMM Memory Module

Caution – Evenly engage the SO-DIMM in its hinge-style slot at the 20-degree angle; uneven contact can cause shorts that will damage the Netra CP2300 board. Do not rock the SO-DIMM into place. Ensure that all contacts engage at the same time. You will feel or hear a “click” when the SO-DIMM properly seats in the connector.

---

4. **Press the top edge of the SO-DIMM toward the board until the retainer clips click into place (see** FIGURE 2-5**).**

   The small metal retainer clips on each side of the SO-DIMM slot are spring-loaded, and will click into place in the notches on the SO-DIMM sides.

2.4.1.2 To Remove a SO-DIMM Memory Module

You may need to remove a SO-DIMM module from the Netra CP2300 board if you are returning the SO-DIMM module or the board for service, or if you are replacing a module with another SO-DIMM module.

Note – Safely store the original factory-shipped SO-DIMM and related SO-DIMM packaging. You may wish to store any removed SO-DIMM in the new SO-DIMM packaging, or use the packaging for service.

To remove a SO-DIMM from the Netra CP2300 board, perform the following steps:

1. **Take antistatic precautions: attach and electrically ground the wrist strap.**

Caution – Always wear a grounded antistatic wrist strap when handling modules.

---

2. **Place the Netra CP2300 board on an antistatic mat, or on the board's antistatic bag if you do not have a mat available.**
3. **For the SO-DIMM you wish to remove, simultaneously pull both SO-DIMM spring retainer clips outward from the slot.**

   The SO-DIMM will release outward at an angle of about 20 degrees (see FIGURE 2-3).

4. **Grasp the SO-DIMM by the edges, and carefully pull it out of its connector. Place it in an antistatic bag.**

   Ensure that you pull the SO-DIMM out at an angle of about 20 degrees, or you may damage the SO-DIMM.

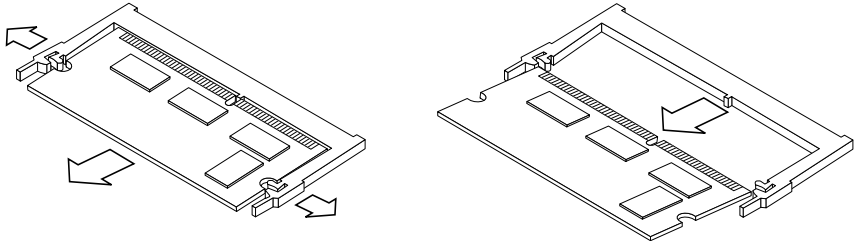

FIGURE 2-3 Removing a SO-DIMM Memory Module

5. **If you are replacing the module you removed with a new SO-DIMM, install it as described in Section 2.4.1.1, "To Install a SO-DIMM Memory Module" on page 2-7.**

2.4.2 Installing Optional PMC Devices

A PCI mezzanine card (PMC) is a slim, modular mezzanine card that provides additional functionality to the Netra CP2300 board. The board contains two PMC slots in which you can install optional PMC devices (see FIGURE 2-1 for the location of these slots). You must install PMC devices on the Netra CP2300 board before you install the board into the chassis.

To provide rear I/O access to the PMC device, the PMC device's ship kit may contain an PIM card that must be installed on the Netra CP2300 transition card. Refer to the PIM card documentation and the *Netra CP2300 cPSB Transition Card Installation and Technical Reference Manual* (816-7188-*xx*) for installation instructions.

Caution – The regular, non-low profile SO-DIMM memory connectors on the CP2300-650-512MB board configuration may interfere with PMC cards installed in PMC slot A, as these tall connectors do not meet the PMC clearance specification (they are 0.5 mm out of clearance). For PMC slot clearance information, see Section A.5.1, "PMC Specification Notes" on page A-6.

2.4.2.1 To Install an Optional PMC Device

Note – The following procedure provides a generic set of instructions for installing PMC devices on the Netra CP2300 board. Refer to the PMC card manufacturer's documentation for specific instructions on installing these devices.

1. **Retrieve the wrist strap from the adapter's ship kit.**
2. **Attach the adhesive copper strip of the antistatic wrist strap to the metal chassis. Wrap the other end twice around your wrist, with the adhesive side against your skin.**
3. **Remove the Netra CP2300 board from its antistatic envelope and place it on an ESD mat (if one is available) near the chassis.**

   If an ESD mat is not available, you can place the card on the antistatic envelope it was packaged in.

Note – If EMI compliance is required, do not remove the PMC filler panel unless you are going to install a PMC to the adapter.

4. **If the PMC has a connector for cabling, remove the Netra CP2300 board's filler panel (**FIGURE 2-4**).**

   Depending on its application, a PMC may contain a connector where you need to attach a PMC-specific cable or it may have LEDs that must be viewed while the operating. If the PMC has a connector or LEDs, remove the board's filler panel so that you can connect the appropriate cable after installing the board.

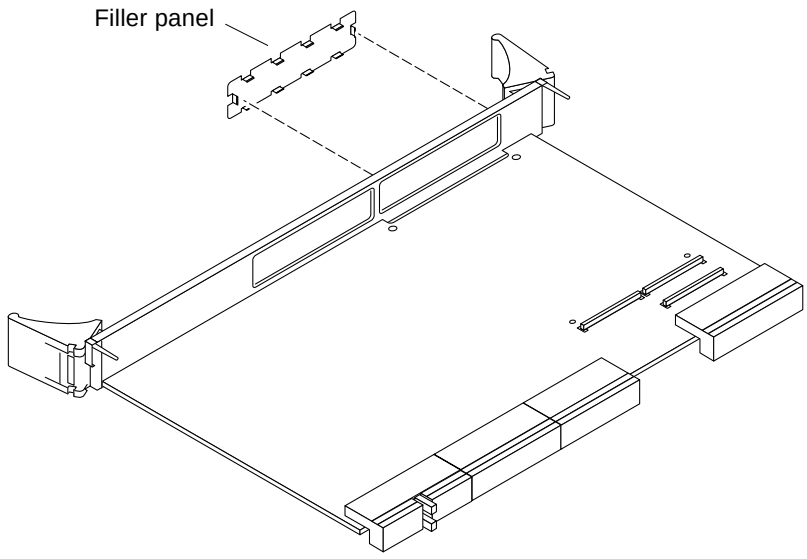

FIGURE 2-4 Removing the PMC Filler Panel

5. **Retrieve the PMC from its ship kit and place it on an antistatic surface.**

6. **Insert the PMC at an angle into the appropriate PMC slot (**FIGURE 2-5**).**

   Make sure that the PMC's connector goes through the board's PMC slot.

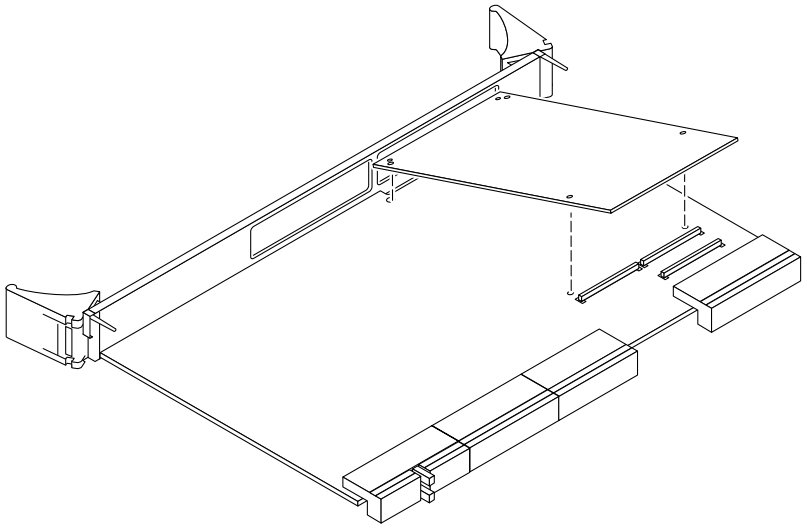

FIGURE 2-5 Inserting the PMC Into the PMC Slot

7. **Align the PMC over the PMC connectors.**
8. **Carefully press the PMC into the board's PMC connectors (**FIGURE 2-6**).**

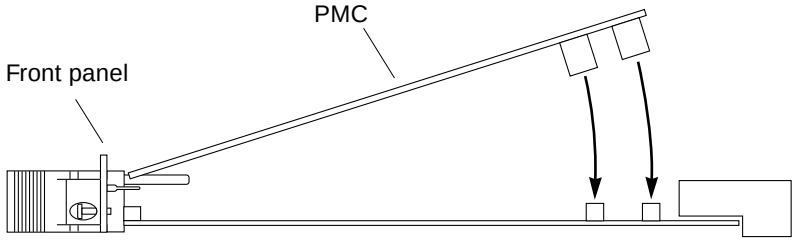

FIGURE 2-6 Pressing the PMC Into the PMC Connectors (Side View)

Caution – Do not use excessive force when installing the PMC into the slot. You may damage the PMC's connectors or the connectors on the Netra CP2300 board, causing permanent damage to the PMC or the board. If the PMC does not seat properly when you apply even pressure, remove the PMC and carefully reinstall it.

9. **Turn the Netra CP2300 board over and use a screwdriver to secure the four screws that attach the PMC to the Netra CP2300 board (**FIGURE 2-7**).**

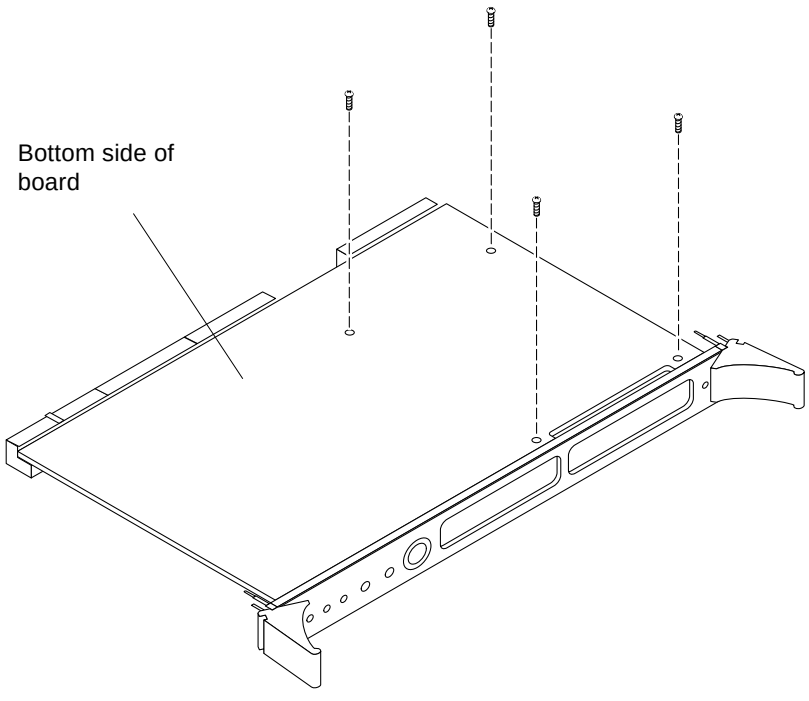

FIGURE 2-7 Securing the PMC Screws

Refer to the PMC device's documentation for PMC software and cabling installation instructions.

2.4.3 Setting Switches

See Section B.5, "DIP Switch Settings" on page B-20 for details about the Netra CP2300 board switch settings.

2.4.4 Replacing the Serial EEPROM

The serial I^{2}C EEPROM stores the board MAC address and host ID information (see Section 5.3.4.4, “Serial I^{2}C EEPROM” on page 5-11 for more information). You do not need to replace the EEPROM unless you are installing a replacement board that does not have the host ID information.

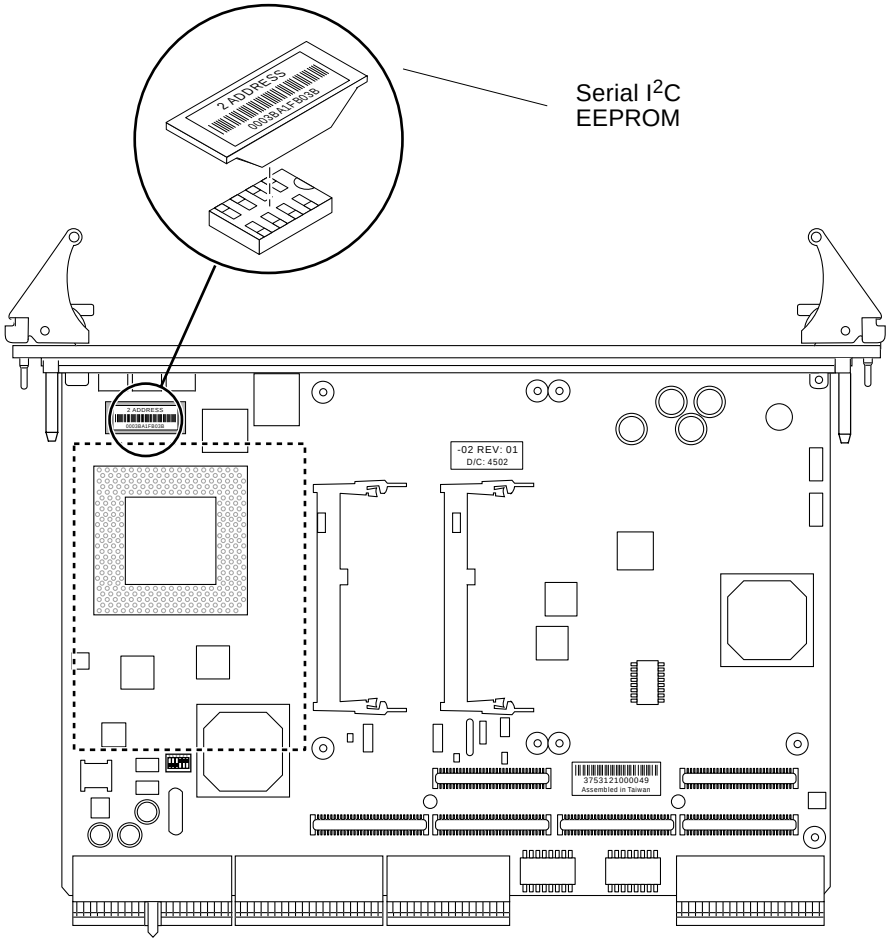

FIGURE 2-8 Replacing the Serial I^{2}C EEPROM

If you need to replace the Netra CP2300 board, remove the serial I^{2}C EEPROM from the original board and install it on the replacement Netra CP2300 board. FIGURE 2-8 shows the position of the serial I^{2}C EEPROM on the Netra CP2300 board. The MAC address label is positioned on top of the serial I^{2}C EEPROM.

2.4.5 Configuring Transition Card Hardware

If you are using the Netra CP2300 transition card, refer to the *Netra CP2300 cPSB Transition Card Installation and Technical Reference Manual* (816-7188-*xx*). You may also want to refer to the transition card manual for detailed connector pin assignments.

2.4.5.1 Installing PIM Assemblies

Follow the PMC card manufacturer's procedure to install PIM cards. Refer to the *Netra CP2300 cPSB Transition Card Installation and Technical Reference Manual* (816-7188-*xx*) for more PIM connector pin assignments and additional installation information.

Caution – When installing a PIM card on to the transition card, ensure that the PIM card power signals match the corresponding power signals of the PIM connectors that are to be installed on the Netra CP2300 cPSB Transition Card.

2.5 Installing Boards Into the cPSB Chassis

This section describes the installation of the transition card, the Netra CP2300 board into a cPSB system chassis.

2.5.1 Installing the Netra CP2300 Transition Card

Refer to the installation procedure detailed in the transition card documentation to install the Netra CP2300 transition card.

Note – If the system power is on when installing the Netra CP2300 transition card, the transition card *must* be installed before its mating Netra CP2300 board.

A compatible transition card must be used with the Netra CP2300 board for rear I/O access. The transition card enables access to the network, to a boot device and to a console terminal. You may use the Netra CP2300 transition card, or you may design your own transition card.

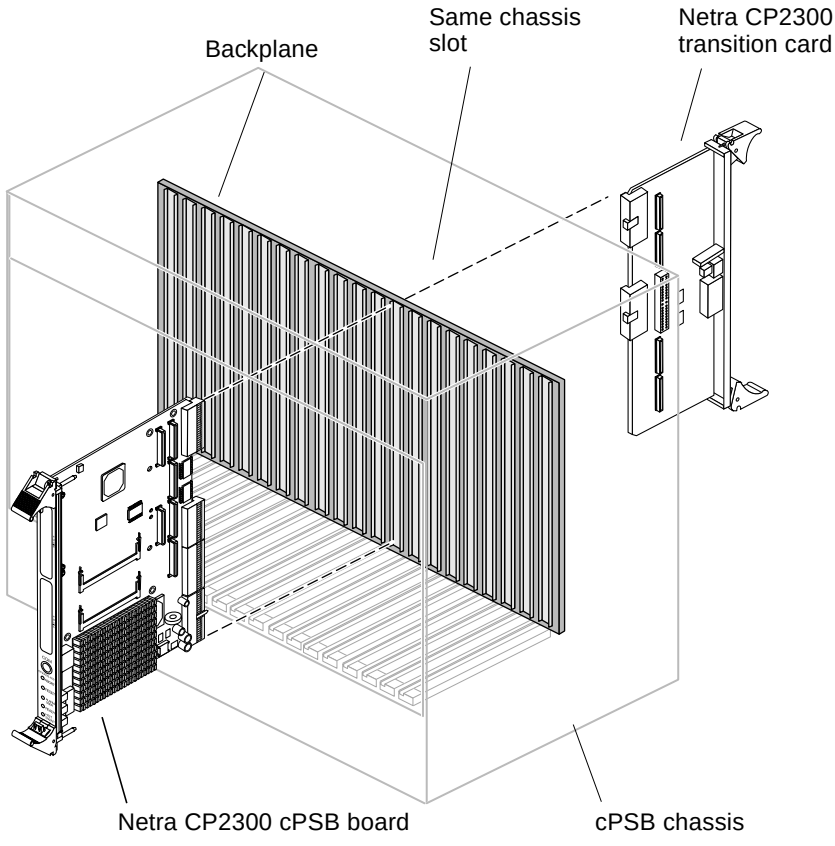

FIGURE 2-9 Installing the Netra CP2300 Transition Card

2.5.2 Installing the Netra CP2300 Board

A cPSB chassis usually contains:

- A system slot. The system slot is indicated by a triangle symbol visible on the backplane, if the chassis meets the PICMG 2.0 CompactPCI specification.
- One or two fabric card slots, which are labelled with a fabric card slot symbol (⋉).
- cPSB Node slots (for a single-segment chassis). Node slots are identified by a circle symbol visible on the backplane.

1. **Ensure that power is disconnected from the chassis.**

   The Netra CP2300 board can be installed while the chassis is powered—however *only start with a powered chassis if necessary.* Check that the corresponding Netra CP2300 transition card is installed.

   If you need a transition card for I/O for the Netra board, ensure that it is already present in the chassis. This step is essential if the chassis is powered during the installation.

2. **Slide the Netra CP2300 board into the appropriate slot on the corresponding top and bottom mounting rails and toward the backplane while gently pushing the board handles inward.**

   While sliding the board, ensure that the Netra CP2300 extraction levers are aligned perpendicular to the card flange in the unlocked position and that the board connectors are aligned with the transition card connectors (FIGURE 2-10).

3. **Install two screws through the top and bottom of the front connector plate to secure the board.**

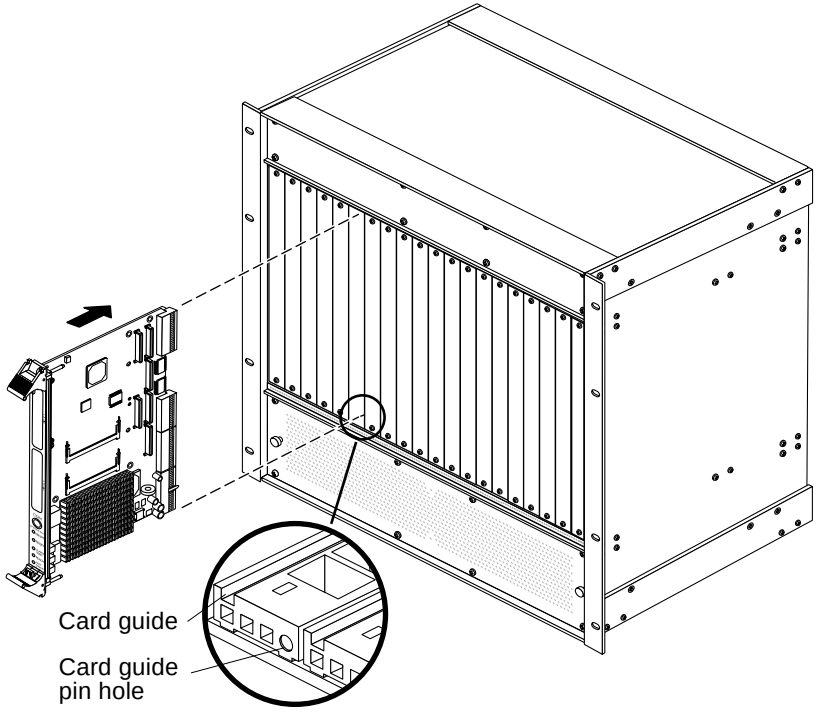

FIGURE 2-10 Installing a Netra CP2300 Board Into a cPSB Chassis Slot

---

Note – Follow the chassis manufacturer's instructions to make sure the Netra CP2300 board is properly installed into the chassis slot.

2.5.3 Installing an I/O Board

Various I/O boards (I/O cards) can be installed in the chassis that contains the Netra board. If these boards meet hot-swap requirements, these can be hot-inserted and do not require that the system is powered down. These I/O cards need to be installed in their respective slots. Refer to the chassis manufacturer's documentation for slot assignments and for special installation instructions.

The basic I/O card installation procedure is the same as described in Section 2.5.2, "Installing the Netra CP2300 Board" on page 2-16. The ejector handles on the I/O cards may not be the same style as Netra board ejector handles. Some boards have retracting ejector handles. Refer to the I/O card manufacturer's instructions on how to engage or disengage ejector handles that secure that board to the chassis.

2.6 Setting Up an Assembled Netra CP2300 Board

This section describes how to set up a computer that contains the Netra CP2300 board.

1. **Using a category 5 grade network cable, connect one RJ45 connector into the receptacle of a chassis Ethernet fabric card or in the receptacle of the Netra CP2300 board's rear transition card.**

   The other end must be connected to a suitable 10/100 Mb Ethernet hub on the local subnet.

   Note – Use shielded cables for Ethernet ports on the transition card. Make sure that the shield is grounded at both ends.

   ---

2. **Connect I/O cabling to the host board and to the serial port of the host system.**
3. **Connect a serial cable to the ttya port on the front panel of the Netra CP2300 board or the Netra CP2300 transition card of the target machine and to the serial port of the host machine.**
4. **Use the `tip` utility on the host system to establish a full-duplex terminal connection with the Netra CP2300 board.**
5. **At the UNIX prompt in a command tool or shell tool, type:**

```
# tip -9600 /dev/ttya
```

6. **Connect any other peripheral devices (such as a printer) to the appropriate connector.**

2.7 Initial Power On and Firmware Upgrade

2.7.1 Powering on the System

Note – In order for the Netra CP2300 board to power on, the cPSB chassis must contain a management controller board.

---

1. **Power on the system that contains the Netra CP2300 board to run the power-on self-tests (POST).**

   For additional details on POST, see Chapter 4.

2. **After running POST, install the Solaris operating environment on the system that contains the Netra CP2300 board.**

   Refer to the *Netra CP2300 cPSB Board Release Notes* (817-1741-*xx*) for information about the software installation and patch information.

2.7.2 Booting From a PMC Disk

If you wish to boot from a PMC disk installed on the Netra CP2300 board, you will need to change the default boot device from the OBP prompt.

To boot from the PMC disk, use the `setenv` command to change the `boot-device` parameter. An example of the `setenv` command and output is shown below.

```
ok setenv boot-device pmcx/disk net
boot-device = pmc0/disk net
ok
```

Where *x* is the number corresponding to the PMC disk that you wish to boot from: `pmc0` corresponds to a disk in the PMC-A slot and `pmc1` corresponds to a disk in the PMC-B slot.

2.7.3 Determining the Firmware Version

If the installed version is not current, update the OpenBoot PROM before continuing (see Section 2.7.4, “Upgrading the OpenBoot PROM Firmware” on page 2-20). The third character group (X) in OpenBoot PROM is the revision number.

2.7.3.1 Determining the Firmware Version From OpenBoot PROM

To determine the installed OpenBoot PROM version, use the `.version` OpenBoot PROM command at the `ok` prompt. An example of the `.version` command output is shown below.

```
ok .version
Firmware version 1.0.0
Firmware CORE Release 1.0.1 created 2002/12/4 14:9
Release 4.0 Version 12 created 2002/11/21 16:18
cPOST version 1.0.0 created 2002/11/25
SMCFW FLASH Code Version 4.0.9 TEST, Spec Version 2.5.2, Platform ID 20
SMCFW BOOT  Code Version 4.15.1
PLD Revision : 1.1
CORE 1.0.1 2002/12/04 14:09
ok
```

2.7.3.2 Determining the Firmware Version From the Solaris Prompt

Use the `prtconf` command at a Solaris terminal prompt to display the firmware version of the board.

```
$ /usr/sbin/prtconf -V
OBP 4.0.15 2003/03/03 16:41 , CORE 1.0.3 2003/01/29 09:21 , cPOST version 1.0.0
created 2002/11/25 , Firmware 1.0.0 , SMCFW 4.0.12
```

2.7.4 Upgrading the OpenBoot PROM Firmware

This firmware can only be upgraded from the OpenBoot PROM `ok` prompt.

1. **Download the latest Netra CP2300 board firmware binaries from the SunSolve web site.**

   For more information about downloading firmware updates, refer to the *Netra CP2300 cPSB Board Release Notes* (817-1741-*xx*). You can download this document from the following web site:

   `http://sun.com/products-n-solutions/hardware/docs/CPU_Boards/`

2. **Bring the system down to OpenBoot PROM level.**

   If your Netra CP2300 board is currently running the Solaris software, become superuser and use the following commands to sync and halt the board:

```
# sync; sync; halt
```

3. **Check the present firmware revision.**

   Check the current firmware revision on the target system by typing:

```
ok .version
```

   A *typical* output is:

```
ok .version
Firmware version 1.0.0
Firmware CORE Release 1.0.1 created 2002/12/4 14:9
Release 4.0 Version 12 created 2002/11/21 16:18
cPOST version 1.0.0 created 2002/11/25
SMCFW FLASH Code Version 4.0.9 TEST, Spec Version 2.5.2, Platform ID 20
SMCFW BOOT  Code Version 4.15.1
PLD Revision : 1.1
CORE 1.0.1 2002/12/04 14:09
ok
```

4. **Disable** `auto-boot?` **configuration variable, and then reset the system.**

   Disable firmware from automatically booting the operating system, and then reset the system using these OpenBoot PROM commands:

```
ok setenv auto-boot? false
ok reset-all
```

5. **Flash update your firmware.**

```
ok flash-update [device;,]<file-path/filepath>
ok smc-flash-update [device;,]<file-path/filepath>
```

If *device* is not specified, then `net` is assumed.

Note – The `flash-update` command will update both the SMC and OpenBoot PROM flash PROMs if both updates are included in the binary file. You can still use the `smc-flash-update` if you want to update the SMC flash only.

The system should automatically reset when the SMC flash update finishes. If it does not, power cycle the Netra CP2300 board.

6. **Check the firmware revision.**

Check the firmware revision by typing:

```
ok .version
```

The form of the output appears as in Step 3. Make sure the version information shows up as expected. If not, attempt the firmware upgrade again.

7. **Re-enable the** `auto-boot?` **configuration variable and reset the system.**

a. Enable auto-booting by typing:

```
ok setenv auto-boot? true
```

b. Reset the system and boot Solaris software by typing:

```
ok reset-all
```

Contact your field service personnel if you encounter any problems when updating the firmware.

Note – Solaris scripts are also available to upgrade core OpenBoot PROM firmware.

CHAPTER 3

Software Configuration

This chapter contains the following sections:

3.1 Hot Swap Information

3.1.1 Hot-Swapping the Netra CP2300 Board

If the Solaris operating environment is up and running on a Netra CP2300 board, and you open the board’s latches, you will see a message that the operating environment will shut down in one minute. When the operating environment drops to the OpenBoot PROM prompt level, you can safely remove the board.

3.1.1.1 Hot-Swap Status LED

The blue hot-swap LED, located on the front panel of the Netra CP2300 board (FIGURE 5-3), lights up when the hot-swap function is enabled by the system software. The hot-swap LED indicates that the board can be extracted from the chassis. When a board is inserted into a cPSB system, the LED is lit automatically until the hardware connection process is completed. The LED then remains off until the extraction is once again enabled by the system software.

FIGURE 3-1 shows how to release the Netra CP2300 handles.

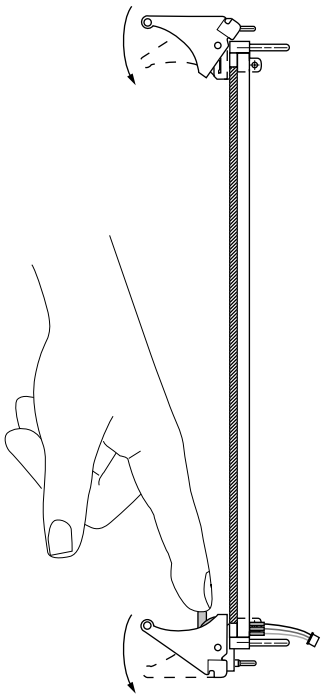

FIGURE 3-1 Releasing the Netra CP2300 Board Handles

3.1.2 Retrieving Device Information

You use the Solaris platform information and control library (PICL) framework for obtaining the state and condition of the Netra CP2300 cPSB board, rather than the Solaris `cfgadm` framework used with other CompactPCI boards.

The PICL framework provides information about the system configuration that it maintains in the PICL tree. Within this PICL tree is a sub-tree named *frutree*, that represents the hierarchy of system FRUs with respect to a root node in the tree called *chassis*. The frutree represents physical resources of the system. The PICL tree is updated whenever a change occurs in a device's status.

The `prtpicl -v` command shows the condition of all devices in the PICL tree. Sample output from the `prtpicl` command related to the Netra CP2300 board is shown below.

```
# prtpicl -v
...
frutree (picl, 4800000301)
 :_class  picl
 :name    frutree
   chassis (fru, 4800000304)
    :ChassisType  SUNW,Netra-CP2300
    :State        configured
    :_class       fru
    :name         chassis
     CPU (location, 4800000309)
      :StatusTime    Sat Mar 29 16:01:26 2003
      :GeoAddr   0x3
      :devfs-path    /pci@1f,0/pci@1
      :bus-addr  1
      :Label     CPU
      :SlotType  pci
      :State     connected
      :_class    location
      :name      CPU
        CPU (fru, 4800000311)
         :ConditionTime   Sat Mar 29 16:01:26 2003
         :StatusTime      Sat Mar 29 16:01:26 2003
         ...
         :Condition   ok
         :State       configured
         :FRUType     bridge/fhs
         :_class      fru
...
```

TABLE 3-1 shows the frutree entries and properties that describe the condition of the Netra CP2300 cPSB board.

TABLE 3-1 PICL FRUtree Entries and Description for the Netra CP2300 cPSB Board

Frutree Entry:Property	Entry Description	Example of Condition
CPU (location) :State	The state of the receptacle, or slot	connected
CPU (fru) :Condition	The condition of the board, or occupant	ok
CPU (fru) :State	The state of the board, or occupant	configured
CPU (fru) :FRUType	The FRU type	bridge/fhs

For more information on the PICL framework, refer to the `picld(1M)` man page.

3.2 Setting the Time of Day

Because the Netra CP2300 board is battery-less, the date and time stored in the TOD chip are not backed up when the system is powered-off. When the system is powered-on, the OpenBoot PROM initializes the date and time fields of the TOD chip. This feature can be configured in different ways in a networked configuration or on a standalone system.

3.2.1 Setting the Time of Day In a Networked Configuration

The Network Time Protocol (NTP) provides the correct timestamp for all systems on a network by synchronizing the clocks of all the systems. A Solaris server, called `xntp`, is queried by OpenBoot PROM for setting and maintaining the timestamp. At least one system or board in the same subnet as the Netra CP2300 must be configured to be an `xntp` server. Refer to the online man pages for the `xntpd`(1M), `ntpq`(`1M`), and `ntpdate`(`1M`) commands for more information about configuring a system to be an xntp server.

The OpenBoot PROM NTP client will be invoked only when system has gone through a hardware power cycle and the configuration variable `ntp-enable?=true` (default value is `false`). The TOD will be programmed with the date and time received from the NTP server.

The configuration variable `ntp-server-addr` can be set with the NTP server's IP address. The default value for `ntp-server-addr` is a broadcast address (`255.255.255.255`). The default value implies that OpenBoot PROM NTP client will broadcast its NTP request in the subnet and update the TOD date and time as per the response received from an NTP server in the subnet.

TABLE 3-2 Values for `ntp-server-addr` Variable

`ntp-server-addr` **Setting**	**Action**
default value	The OpenBoot PROM NTP client will broadcast its NTP request in the subnet.
NTP server's IP address	The OpenBoot PROM NTP client will send the NTP request to the NTP server

If `ntp-enable?=false`, OpenBoot PROM will not invoke its NTP client and the TOD will be programmed with a `1/1/2000` date and the time will be set to start at 00:00:00 hours.

TABLE 3-3 Values for `ntp-enable?` Variable for Networked Configuration

`ntp-enable?` **Setting**	**Action**
`false`	OpenBoot PROM will not invoke its NTP client and programs the TOD with the 1/1/2000 date.
`true`	OpenBoot PROM sends an NTP request and programs the TOD with the response from NTP server. In case of any failure, OpenBoot PROM will program the TOD with the 1/1/2000 date and 00:00:00 time.

To use the NTP feature at Solaris level, configure the NTP client at the Solaris level.

For information on setting OpenBoot PROM configuration variables, see the Section 4.2.2, "OpenBoot PROM Configuration Variables" on page 4-8.

3.2.2 Setting the Time of Day on a Standalone System

On a standalone, battery-less system, which cannot get the time of day from a network source, the TOD will be programmed with the default date and time of 1/1/2000 00:00:00 GMT. The `ntp-enable` variable should be `false`, but even if it is set to `true`, the NTP request will time out after one minute, and the TOD will be programmed with the default date and time of 1/1/2000 00:00:00 GMT.

- **To set the time of day manually after the power is restored:**

  As superuser, use the `date` command at a Solaris prompt to set the correct time.

```
# date [mmddHHMMccyy]
```

  Where:

  - *mm* is the current month.
  - *dd* is the current day of the month.
  - *HH* is the current hour of the day.
  - *MM* is the current minutes past the hour.
  - *cc* is the current century minus one.
  - Century (a year divided by 100 and truncated to an integer) as a decimal number [00-99]. For example, cc is 19 for the year 1988 and 20 for the year 2007.
  - *yy* is the current year.

  Refer to the `date(1M)` command man page for additional information. After you set the date, you must reboot (but not power cycle) the system for the changes to take full effect. Failing to reboot can cause time conflicts among applications.

3.3 Downloading and Installing SunVTS

The Sun Validation Test Suite (SunVTS™ software) is a comprehensive software package that tests and validates the Netra CP2300 by verifying the configuration and function of most hardware controllers and devices on the board. SunVTS is used to validate a system during development, production, inspection, troubleshooting, periodic maintenance and system or subsystem stressing. SunVTS can be tailored to run on various types of machines ranging from desktops to servers with modifiable test instances and processor affinity features.

You can perform high-level system testing by using the appropriate version of SunVTS. For detailed information on SunVTS support and downloads, refer to the following web site:

`http://www.sun.com/oem/products/vts/`

The SunVTS packages are also located on the Solaris 8 Supplemental Software CD for Sun Computer Systems that ships with the Solaris operating environment release.

Ensure that the SunVTS software version is compatible with the Solaris operating environment version being used. Solaris 8 2/02 operating environment is compatible with SunVTS 4.6 package.

Information on the version of the SunVTS software installed can be found in the file:

`/opt/SUNWvts/bin/.version`

To obtain SunVTS documentation, contact your local customer service representative or field application engineer.

Note – For security reasons only a superuser is permitted to run SunVTS. Installation and starting instructions are included with the software when it is downloaded.

CHAPTER 4

Firmware

The Netra CP2300 board contains a modular firmware architecture that gives you latitude in controlling boot initialization. You can customize the initialization, test the firmware, and even enable the installation of a custom operating system.

This platform also employs the System Management Controller (SMC)—described in Section 5.6, “System Management Controller” on page 5-21—which controls the system management and hot-swap control, and some board hardware. The SMC configuration is controlled by separate firmware.

This chapter contains the following sections:

4.1 Firmware Initialization

Control flow at board startup is shown in FIGURE 4-1. Execution begins in Firmware Common Operations and Reset Environment (CORE)—which includes Basic POST (BPOST). It passes to Comprehensive POST (CPOST) and Extended POST (EPOST), if these are present, before returning to firmware CORE and on to OpenBoot PROM. The test execution path is determined by environment variables.

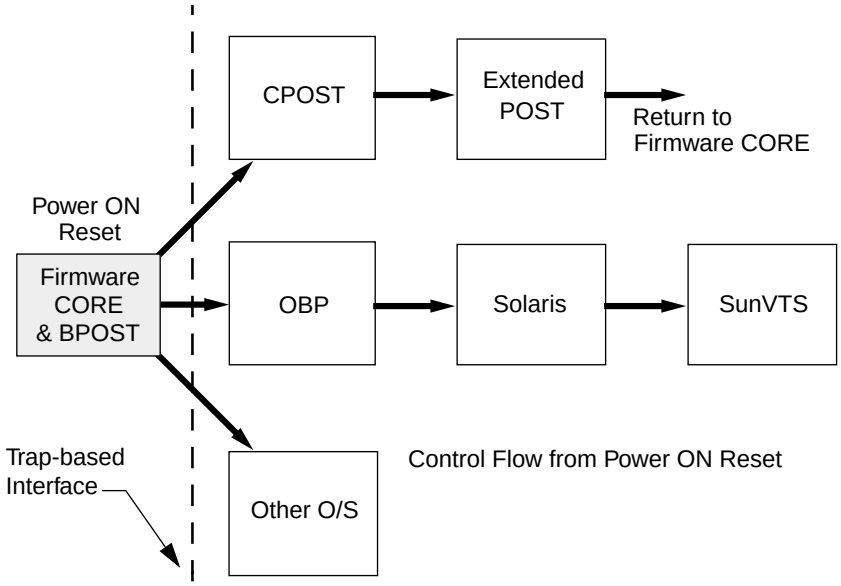

FIGURE 4-1 Control Flow from Power On for Firmware CORE and Client Modules—Solaris Case

4.1.1 Firmware CORE and BPOST

Firmware CORE provides the following functionality:

- Unifies system initialization and I/O operations for a higher-level client, for example, OpenBoot PROM for Solaris software
- Avoids any duplication of effort for the same type of functions among various clients
- Provides a unified interface to higher level software using a soft-trap mechanism. Trap services (software interrupts) are used to abstract hardware-dependent features behind a uniform service interface. Sun SPARC™ processors are designed with a common software trap structure that is useful for this common

programming interface, so that clients may not need to carry another copy of those drivers and may use those services provided by firmware CORE until their driver takes over.

- Provides access, early in the boot sequence, to the hardware-dependent services needed for client initialization. Examples are I/O devices, such as serial port and network.
- Provides basic system tests that can replace existing POST in `min mode`.
- Enables extensive system testing to be done using the POST dropin in `max mode`.
- Provides error recovery from exceptions that currently does not exist in OpenBoot PROM.
- Enables use of popular languages with efficient compilation and easier debugging for development

BPOST is integrated into firmware CORE. BPOST tests are interleaved with the initialization activities of firmware CORE to present a foundation of validated and initialized hardware to run subsequent code such as that in CPOST or OpenBoot PROM. The tests listed in TABLE 4-1 are examples of CORE and BPOST flow of execution.

Note – Not all of the hardware listed in this table is present on this platform. When a hardware item is not detected by the firmware, this firmware makes no attempt to test or initialize it.

Because BPOST runs from PROM, its extent of testing is limited to that needed by modules that are loaded later. Such a module, for example CPOST, can perform comprehensive testing more quickly because it executes from DRAM.

TABLE 4-1 Firmware CORE and BPOST Flow of Execution

Firmware CORE Service	Description
Initialize processor	Sets processor in stable state.
Initialize NVRAM	Sets up state variables.
Initialize XBus and bridges	Initializes XBus and UPA/PCI and PCI/PCI bridges in path between CPU and XBus devices.
Initialize TTY	For message display.
Set memory timings	
Verify NVRAM	Check magic number. Set defaults if bad.
Check keyboard	Probe & initialize keyboard, set TTYA otherwise.
Check I/O device for key pressed	Set state variables in NVRAM accordingly.

TABLE 4-1 Firmware CORE and BPOST Flow of Execution *(Continued)*

Firmware CORE Service	Description
Cache, MMU test	Perform basic diagnostics on caches & MMUs*.
Initialize caches, MMUs	Setup I and D caches and MMUs.
Memory probe	Probe memory and clear top memory region.
Memory test	Perform partial memory test†.
MMU and cache setup	Setup I/D MMUs with valid mappings; enable MMUs and I/D caches.
Copy firmware CORE	Copy firmware CORE into memory and transfer control to the RAM copy.
Set up trap table	Set up trap table in memory.
Initialize interrupts	Set up hardware interrupts.
Initialize TOD	Initialize the time of day.
Set up CPU counter	Calibrate CPU counter to determine module speed.
Execute POST dropin†	
Locate the client	Locate the client in PROM. If found, copy into memory and transfer control to it.
Enter user interface	OpenBoot PROM for Solaris software, else RTOS or custom OS.

* Execute if hardware `power-on`, `diag-switch?` set to `true`, `diag-level` set to `min/max`, and key to skip POST not pressed.

† Execute if hardware power-on, `diag-switch?` set to `true`, `diag-level` set to `max` and key to skip POST not pressed.

4.1.2 CPOST and EPOST

CPOST contains tests for higher-level board functions. By placing these tests in a separate module, the user has the option of performing them and the developer can substitute them with other tests. Examples of CPOST tests are:

- PCI configuration register test for PCIO-2
- DMA tests
- SMC test

4.1.3 EPOST

EPOST is used for additional POST code dropins that are provided by the user.

4.1.4 OpenBoot PROM

Rather than executing the initialization code that formerly existed in OpenBoot PROM for prior Sun board platforms, OpenBoot PROM now makes calls to the traps laid down by firmware CORE. OpenBoot PROM exists in the form of a dropin in the system flash memory area.

OpenBoot PROM probes for devices and builds the device tree, which is a table that contains entries for how drivers communicate with connected hardware. Each line, or entry, of the device tree is a reference for the node entry for the peripheral in the `/dev` directory. The device tree is inherited by Solaris software as it is booted. An example of a device tree is shown below. The device tree can be seen by directory in the `/` directory. The device tree can be seen by typing `show-devs` at the `ok` prompt. An example of a device tree appears below.

CODE EXAMPLE 4-1 OpenBoot PROM `show-devs` Command Output

```
ok show-devs
/SUNW,UltraSPARC-IIe@0,0
/pci@1f,0
/ssp-serial
/multiplexer@0,0
/virtual-memory
/memory@0,0
/aliases
/options
/openprom
/chosen
/packages
/pci@1f,0/pci@1
/pci@1f,0/pci@1,1
/pci@1f,0/pci@1,1/usb@a
/pci@1f,0/pci@1,1/ide@d
/pci@1f,0/pci@1,1/ethernet@2
/pci@1f,0/pci@1,1/ethernet@1
/pci@1f,0/pci@1,1/pmu@3
/pci@1f,0/pci@1,1/isa@7
/pci@1f,0/pci@1,1/ide@d/cdrom
/pci@1f,0/pci@1,1/ide@d/disk
/pci@1f,0/pci@1,1/pmu@3/gpio@80000000,8a
/pci@1f,0/pci@1,1/pmu@3/i2c@0,0
/pci@1f,0/pci@1,1/pmu@3/i2c@0,0/i2c-nvram@0,8e
/pci@1f,0/pci@1,1/pmu@3/i2c@0,0/i2ctod@0,b0
/pci@1f,0/pci@1,1/pmu@3/i2c@0,0/dimm@0,70
/pci@1f,0/pci@1,1/pmu@3/i2c@0,0/dimm@0,80
/pci@1f,0/pci@1,1/pmu@3/i2c@0,0/dimm@0,88
/pci@1f,0/pci@1,1/pmu@3/i2c@0,0/i2c-nvram@0,8e/idprom@1fd8
```

CODE EXAMPLE 4-1 OpenBoot PROM `show-devs` Command Output *(Continued)*

```
/pci@1f,0/pci@1,1/isa@7/sysmgmt@0,8010
/pci@1f,0/pci@1,1/isa@7/flashprom@1f,100000
/pci@1f,0/pci@1,1/isa@7/flashprom@1f,0
/pci@1f,0/pci@1,1/isa@7/serial@0,2e8
/pci@1f,0/pci@1,1/isa@7/serial@0,3f8
/pci@1f,0/pci@1,1/isa@7/power@0,2000
/pci@1f,0/pci@1,1/isa@7/dma@0,0
/openprom/client-services
/packages/kbd-translator
/packages/console-pkg
/packages/dropins
/packages/SUNW,builtin-drivers
/packages/cdfs
/packages/ufs-file-system
/packages/disk-label
/packages/obp-tftp
/packages/deblocker
/packages/terminal-emulator
ok
```

The OpenBoot PROM also contains aliases for some of the devices shown in the device tree. These aliases can simplify hardware access at the ok prompt. CODE EXAMPLE 4-2 shows how the OpenBoot `devalias` command lists the available device tree aliases.

CODE EXAMPLE 4-2 OpenBoot PROM `devalias` Command Output

```
ok devalias
output-mux        /multiplexer:output
input-mux         /multiplexer:input
ssp-serial        /ssp-serial
hsc               /pci@1f,0/pci@1,1/isa@7/sysmgmt@0,8010
pmc1              /pci@1f,0/pci@1/@2
pmc0              /pci@1f,0/pci@1/@1
rtc               /pci@1f,0/pci@1,1/pmu@3/i2c@0,0/i2ctod@0,b0
usb               /pci@1f,0/pci@1,1/usb@a
uflash            /pci@1f,0/pci@1,1/isa@7/flashprom@1f,100000
flash             /pci@1f,0/pci@1,1/isa@7/flashprom@1f,0
systemprom        /pci@1f,0/pci@1,1/isa@7/flashprom@1f,0
i2c-nvram         /pci@1f,0/pci@1,1/pmu@3/i2c@0,0/i2c-nvram@0,8e
dload2            /pci@1f,0/pci@1,1/ethernet@2:,
net2              /pci@1f,0/pci@1,1/ethernet@2
dload             /pci@1f,0/pci@1,1/ethernet@1:,
```

CODE EXAMPLE 4-2 OpenBoot PROM `devalias` Command Output *(Continued)*

```
net                 /pci@1f,0/pci@1,1/ethernet@1
cdrom               /pci@1f,0/pci@1,1/ide@d/cdrom@2,0:f
disk                /pci@1f,0/pci@1,1/ide@d/disk@0,0
disk3               /pci@1f,0/pci@1,1/ide@d/disk@3,0
disk2               /pci@1f,0/pci@1,1/ide@d/disk@2,0
disk1               /pci@1f,0/pci@1,1/ide@d/disk@1,0
disk0               /pci@1f,0/pci@1,1/ide@d/disk@0,0
ide                 /pci@1f,0/pci@1,1/ide@d
floppy              /pci@1f,0/pci@1,1/isa@7/dma/floppy
ttyb                /pci@1f,0/pci@1,1/isa@7/serial@0,2e8
ttya                /pci@1f,0/pci@1,1/isa@7/serial@0,3f8
ok
```

4.2 Firmware Configuration Variables

This section provides some information on the CORE SRAM variables and the configuration variables. Firmware configuration variables are saved in the 8 Kbyte I^2C serial EEPROM. The EEPROM's contents are preserved across board power-cycles.

4.2.1 Firmware CORE Execution Control

The key combinations listed in TABLE 4-2 can be used to control the flow of execution at system boot. These key combinations must be pressed when you turn the power on.

TABLE 4-2 Key Sequences

Key combination	Result
Control-P	Skip POST
Control-N	Set default SRAM configuration variables
Control-M	Sets `diag-switch?` to true (see TABLE 4-4)
Control-U	Enter CORE user interface

The Netra CP2300 boards support USB keyboards.

4.2.2 OpenBoot PROM Configuration Variables

TABLE 4-3 describes the OpenBoot PROM configuration variables stored in the NVRAM and displayed by the OpenBoot PROM `printenv` command. Use the `setenv` OpenBoot command to modify the environment variables. The boot process is controlled by several variables (see TABLE 4-4). For values of each variable, refer to the *OpenBoot 4.x Command Reference Manual* (see Appendix D).

TABLE 4-3 OpenBoot PROM SRAM Configuration Variables

Variable Name	Default Value	Description
`multiplexer-output-devices`	`ttya ttye`	`Specify multiple output devices.`
`multiplexer-input-devices`	`ttya ttye`	`Specify multiple input devices.`
`dhcp-clientid`		`Specifies the client information needed for a DHCP boot.`
`shutdown-temperature`	`91`	Sets the CPU shutdown temperature.
`critical-temperature`	`79`	Sets the CPU critical temperature.
`warning-temperature`	`74`	Sets the CPU warning temperature.
`env-monitor`	`enabled`	Enable or disable environment monitoring at the OpenBoot PROM.
`ntp-server-addr`	`255.255.255.255`	Network time protocol (NTP) internet address.
`ntp-enable?`	`false`	Enable NTP synchronization.
`diag-passes`	`1`	Repeats each diagnostic test the number of times specified.
`diag-continue?`	`0`	When false, the diagnostic testing will stop within a test routine and prints a message as soon as an error is detected. After printing the message, the testing will then skip to the next test routine in the sequence. When true, the diagnostic testing will run all subtests within a test, even if an error is detected.
`diag-targets`	`0`	Specify the target of the diagnostic testing.
`diag-verbosity`	`0`	Sets the level of diagnostic messages: • `0` = Prints one line that indicates the device being tested and its pass/fail status. • `1` = Prints more detailed test status, which varies in content from test to test. • `2` = Prints subtest names. • `4` = Prints debug messages. • `8` = Prints back trace of callers on error.

TABLE 4-3 OpenBoot PROM SRAM Configuration Variables *(Continued)*

Variable Name	Default Value	Description
post-on-sir?	false	If variable is set to true, execute POST on soft reset.
keyboard-click?	false	If variable is set to true, enable keyboard click sound.
keymap		Use key map for custom keyboard.
scsi-initiator-id	7	Sets the SCSI bus address of host adapter, with a range of 0-7.
#power-cycles	No default	Initialized by manufacturer.
system-board-serial#	No default	Initialized by manufacturer.
system-board-date	No default	Initialized by manufacturer.
ttyb-rts-dtr-off	false	If variable is set to true, the operating system does not assert DTR and runs on TTYB.
ttyb-ignore-cd	true	If variable is set to true, the operating system ignores TTYB carrier-detect.
ttya-rts-dtr-off	false	If variable is set to true, the operating system does not assert DTR and runs on TTYA.
ttya-ignore-cd	true	If variable is set to true, the operating system ignores TTYA carrier-detect.
ttyb-mode	9600,8,n,1,-	TTYB settings (baud, #bits, parity, #stop, handshake).
ttya-mode	9600,8,n,1,-	TTYA settings (baud, #bits, parity, #stop, handshake).
pcia-probe-list	1,2	Probe list of devices present on internal PCI bus A.
pcib-probe-list	7,3,1,2,d,a	Probe list of devices present on internal PCI bus B.
mfg-mode	off	Manufacturing test mode (leave off).
diag-level	max	Sets the level of diagnostics to run (max or min).
watchdog-timeout	65535	Watchdog timeout value (in 1/10 sec.)
watchdog-enable?	false	Enable programming of watchdog
fcode-debug?	false	OpenBoot PROM dedub variable.
output-device	ttya	Console output device (usually a screen, TTYA, or TTYB).
input-device	ttya	Input device used at power-on (usually keyboard, TTYA, or TTYB).
load-base	16384	Base address where the client image is loaded by the OpenBoot PROM.

TABLE 4-3 OpenBoot PROM SRAM Configuration Variables *(Continued)*

Variable Name	Default Value	Description
auto-boot-retry?	false	Attempt to reboot if initial boot fails.
boot-command	boot	Command that is executed if auto-boot? is set to true.
auto-boot?	true	If variable is set to true, the board boots automatically after a power-on reset.
watchdog-reboot?	false	If variable is set to true, the board boots automatically after a watchdog reset.
diag-file		File from which to boot in diagnostic mode.
diag-device	net	Device from which to boot.
boot-file		File from which to boot (an empty strings lets the secondary boot choose the default).
boot-device	disk net	Device from which to boot.
net-timeout	0	Specify the retry time to boot from the network. After timeout, the boot will abort. The default setting is 0 (retry infinite times).
ansi-terminal?	true	This variable is not applicable.
screen-#columns	80	Screen width in columns.
screen-#rows	34	Screen height in rows.
local-mac-address?	false	If variable is set to true, network drivers use the board's MAC address, and not the system's address.
silent-mode?	false	If variable is set to true, suppress messages related to clearing memory.
use-nvramrc?	false	If variable is set to true, execute commands in NVRAMRC during the board start-up.
nvramrc		Contents of the NVRAMRC.
security-mode	No default	Firmware security level (none, command, or full). • none: no password required. • command: all commands except for boot and go require password. • full: all commands except for go require password.
security-password	No default	Set the firmware security password (never displayed).
security-#badlogins	No default	OpenBoot PROM internal use.

TABLE 4-3 OpenBoot PROM SRAM Configuration Variables *(Continued)*

Variable Name	Default Value	Description
oem-logo	No default	Byte array custom OEM logo (enabled by oem logo? true); displayed in hex.
oem-logo?	false	If true, use custom OEM logo, else use Sun logo.
oem-banner	No default	Custom OEM banner (enabled by oem-logo? true).
oem-banner?	false	If variable is set to true, use custom OEM banner.
hardware-revision	No default	Initialized in manufacture.
last-hardware-update	No default	Initialized in manufacture.
diag-switch?	false	If variable is set to true, POST is executed when system is next powered.

The diag-switch? and diag-level variables listed in TABLE 4-3 affect the path through the various embedded tests. TABLE 4-4 shows the effect of setting these variables.

BPOST is embedded within the firmware CORE and is executed when the OpenBoot PROM environment variable, diag-switch? is set to true and diag-level set to min. Similarly CPOST (and EPOST if it is present) is executed when diag-level is set to max. The permutations are shown in TABLE 4-4.

TABLE 4-4 OpenBoot PROM Variable Settings for Executing the POST Modules

Module	diag-switch? Setting	diag-level Setting	Description
BPOST	false	X	No messages are output to TTY.
	true	max (0x40)	Runs BPOST.
	true	min (0x20)	Runs BPOST.
	true	off (0x0)	No POST executed; messages displayed on TTYa.
CPOST	false	X	No messages are output to TTY.
	true	max (0x40)	Runs after BPOST.
	true	min (0x20)	CPOST is not run.
	true	off (0x0)	No POST executed; messages displayed on TTYa.

TABLE 4-4 OpenBoot PROM Variable Settings for Executing the POST Modules

Module	`diag-switch?` Setting	`diag-level` Setting	Description
EPOST	false	X	No messages are output to TTY.
	true	max (0x40)	Runs automatically after CPOST (if EPOST module is present).
	true	off (0x0)	No POST executed; messages displayed on TTYa.

4.3 System Flash PROM Memory Map

The node board boots from the 1 Mbyte system flash PROM device, which contains the firmware CORE, basic POST code, comprehensive POST, and OpenBoot PROM. The contents map of this PROM is shown in FIGURE 4-2.

User-developed code can also be programmed into the user flash memory space in the form of *dropins*. The system flash can be upgraded by running a program out of OpenBoot PROM—see Section 4.6, “SMC Firmware” on page 4-18. It is not otherwise accessible by the user.

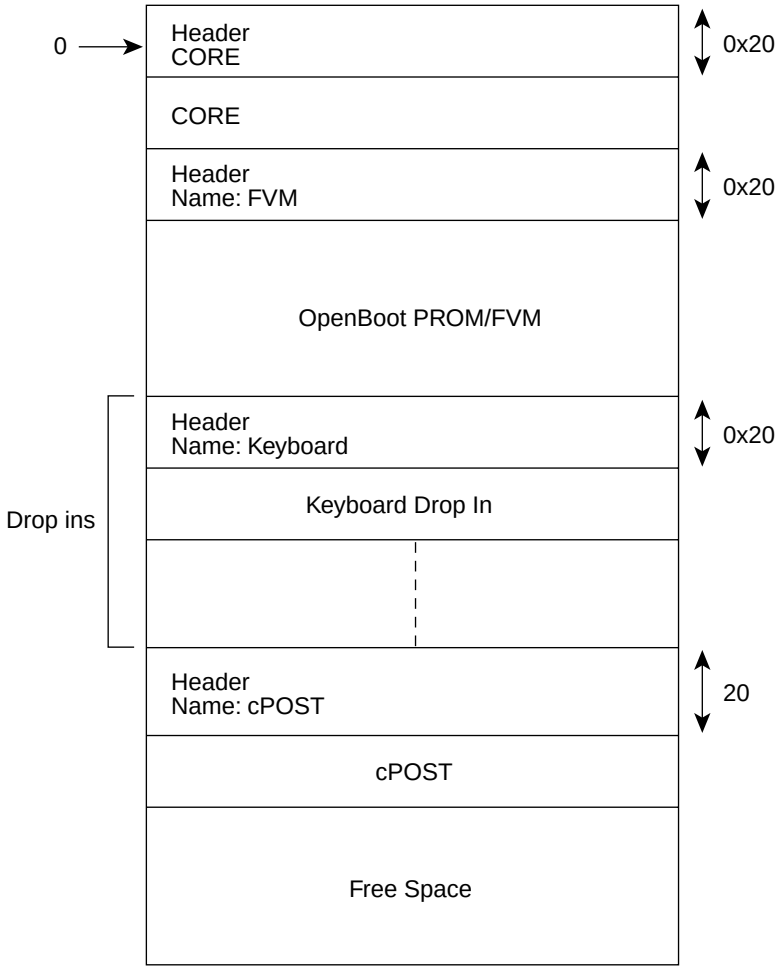

FIGURE 4-2 System Flash PROM Map

4.4 USB Keyboard Support

The Netra CP2300 supports USB keyboards only.

4.5 Environmental Monitoring Support at OpenBoot PROM

The Netra CP2300 board has an intelligent fault detection environmental monitoring system to increase uptime and manageability at OpenBoot PROM. The SMC module on the Netra CP2300 board supports the temperature monitoring functions. Environmental monitoring tracks the following at regular intervals at the `ok` prompt:

- CPU heat sink thermal sensor
- Ejection switch
- ENUM signal

Note – Refer to the *Netra CP2300 cPSB Board Programming Guide* (817-1331-*xx*) for additional information about the environmental monitoring features of the Netra CP2300 board.

4.5.1 CPU Thermal Sensor

At the OpenBoot PROM level, when an over-temperature condition occurs, corresponding messages are displayed on the console. The OpenBoot PROM displays the warning messages as soon as the board temperature reaches the warning temperature and is still below the critical temperature. The critical messages are displayed as soon as the board temperature reaches the critical temperature. Finally, the shutdown messages are displayed when the board temperature reaches the shutdown temperature.

The `warning-temperature`, `critical-temperature`, and `shutdown-temperature` are maintained in the SRAM for the Netra CP2300 board (for default warning, critical, and shutdown temperature values, see TABLE 4-3). Also, the `show-sensors` command at OpenBoot PROM displays the readings of all the temperature sensors on the board.

When the CPU temperature reaches the set warning temperature limit, the following message is displayed at the `ok` prompt at regular intervals:

```
<<< !!! ALERT!!! Upper Non-critical - going high >>>
     The current threshold setting is:  < >
     The current temperature is      : < >
```

When the CPU temperature reaches the set critical temperature limit, the following message is displayed at the ok prompt at regular intervals:

```
<<< !!! ALERT!!! Upper Critical - going high >>>
     The current threshold setting is:  < >
     The current temperature is      : < >
```

The warning, critical, and shutdown temperature values provided are the OpenBoot PROM default values. A user can change these values by changing the corresponding SRAM variable values and resetting the system hardware or software.

```
ok setenv env-monitor enabled
ok setenv warning-temperature  <new_value>
ok setenv shutdown-temperature <new_value>
ok setenv critical-temperature <new_value>
ok reset-all
```

The *<new_value>* is a decimal value for a new temperature limit. The OpenBoot PROM then uses the new temperature limits after the system reset.

Caution – Be careful when setting the temperature parameters. Setting the warning-temperature and shutdown-temperature values too high will leave the system unprotected against overheating. Setting the temperature too low may cause the Netra CP2300 board to send error messages continuously.

4.5.2 Reading the CPU Temperature and OpenBoot PROM Temperature Limits

You can access the CPU temperature sensor current readings and environmental monitoring settings from the Solaris prompt by typing the following commands. Sample output is listed after each command.

`prtpicl` command example:

```
# prtpicl -v -c temperature-sensor
CPU-sensor (temperature-sensor, 36000005ce)
  :State         ok
  :HighWarningThreshold   74
  :HighShutdownThreshold  79
  :HighPowerOffThreshold  91
  :LowWarningThreshold   -10
  :LowShutdownThreshold  -13
  :LowPowerOffThreshold  -20
  :Temperature   53
  :GeoAddr       0xe
  :Label         Ambient
  :_class        temperature-sensor
  :name  CPU-sensor
```

`prtdiag` command example:

```
# prtdiag -v

CPU Node Temperature Information
--------------------------------

Temperature Reading: 53
Critical Threshold Information
------------------------------
High Power-Off Threshold           91
High Shutdown Threshold            79
High Warning Threshold             74
Low Power Off Threshold           -20
Low Shutdown Threshold            -13
Low Warning Threshold             -10
```

`eeprom` command example:

```
# eeprom | grep temp
shutdown-temperature=91
critical-temperature=79
warning-temperature=74
```

TABLE 4-5 shows which Solaris commands and values correspond to the environmental monitoring warning that runs when the CPU temperature exceeds the set limit.

TABLE 4-5 Description of Values Displayed by Solaris Commands

Environmental Monitoring Warning	`prtpicl`	`prtdiag`	`eeprom`
The first-level temperature warning is displayed.	`HighWarning Threshold`	`High Warning Threshold`	`warning-temperature`
The second-level temperature warning is displayed.	`HighShutdown Threshold`	`High Shutdown Threshold`	`critical-temperature`
The CPU shutdown message is displayed and the CPU is shut off.	`HighPowerOff Threshold`	`High Power-Off Threshold`	`shutdown-temperature`

4.6 SMC Firmware

The field upgradeable SMC firmware supports features such as Netra CP2300 resources, temperature monitoring, control of the power subsystem, IPMI communication with other boards, configurable reset handling, hot-swap capability, and watchdog timer heartbeat mechanism. The SMC firmware also has its own built-in self-test at power up. The SMC consists of DS80CH11, which is an 8051 compatible chip and the PSD833F2 memory chip. Inside the PSD833F2 chip, there are the main flash and the boot flash and SRAM for data storage. The host CPU sends commands and data to SMC by way of the SBus. For more details on the SMC subsystem see Section 5.6, “System Management Controller” on page 5-21.

The SMC architecture allows the update of the SMC firmware. SMC firmware is only updated from the OpenBoot PROM. This feature is used to modify SMC firmware during a field upgrade, for fixing bugs, adding enhancements or new features, or providing special code for a specific OEM customer.

The SMC is capable of performing a flash update on the main and boot flash memory. The main flash can flash update the boot flash, and the boot flash can flash update the main flash. The boot code contains the minimum code to enable the system to boot to the `ok` prompt if the main flash fails, and to switch from boot flash to main flash for execution. Therefore, any attempt to perform a flash update of the boot flash would be considered risky and should not be done often.

The CORE/OpenBoot PROM code has support for recovery if the SMC flash update fails. When it detects that SMC is running from boot code, the code automatically goes to the `ok` prompt, enabling you to perform a flash update. Commands other than `flash-update` and `get-version` are not supported while running from the boot code.

Note – Due to interdependency between OpenBoot PROM CORE, SMC and hardware, you must take into account compatibility between various parts of the system among different version numbers when performing flash update.

4.6.1 SMC Configuration Block

The SMC power-on behavior and other attributes are stored in a 16-byte configuration block. This configuration block is stored in an accessible serial I^2C SEEPROM. In the absence of this configuration block, SMC boots up in a default mode. At the OpenBoot PROM level, the `setsmcenv` and `printsmcenv` commands

in the SMC node are used to set parameters in the configuration block of SMC. The `printsmcenv` command prints the value of the parameters in the SMC configuration block.

4.6.1.1 Setting the SMC Configuration Block

To view the settings on the configuration block, read the block using the `printsmcenv` command. If you want to change the settings, use the `setsmcenv` command to change the SEEPROM configuration block. Some examples are given in the code example below.

```
ok printsmcenv
config-version         : 1
backplane-type         : 0
reset-action           : 66
sir-xir-enable         : 2
back-end-power-option  : 0
chassis-type           : 0
flash-device           : 0
set-role-option        : 0
ipmi-checksum-ctlr     : 1
healthy-option         : 0
byteB                  : 0
byteC                  : 0
byteD                  : 0
byteE                  : 0
byteF                  : 0
byte10                 : 0
ok setsmcenv flash-device 4
ok
```

Note – Each setting on the configuration block can change the behavior of the board significantly. For example, an invalid value in `config-version` would cause the OpenBoot PROM to reset the configuration block to the default values. Ask your Sun field application engineer for further details on the configuration block settings.

4.7 Updating Flash PROMs

On the Netra CP2300 board, both the system (boot) flash and the user flash memory reside on the same physical device. By default the system flash uses 1 MByte of flash memory while the user flash uses 7 MBytes of flash memory (TABLE 4-4). For more information about system flash and user flash memory, see Section 5.3.4, “Memory Components” on page 5-10.

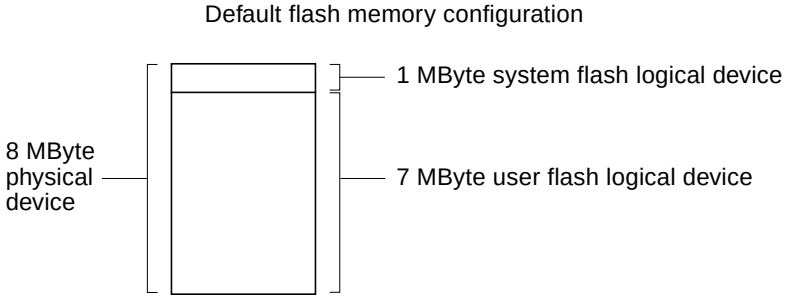

FIGURE 4-3 System Flash and User Flash Logical Devices on Same Physical Device

4.7.1 Exchanging the System and User Flash Memory Devices

By default, the system flash is allocated 1 MByte of memory and user flash is allocated 7 MBytes of memory. If your application environment requires it, you can exchange these logical memory devices and make the system flash use 7 MBytes of memory and the user flash 1 MByte of memory.

To exchange these memory allocations, you must first change the SW3 DIP switch setting and set the `flash-device` setting in the configuration block. (See Section 4.6.1, “SMC Configuration Block” on page 4-18 for more information about the configuration block.)

To Exchange the Flash Memory Devices:

1. **At the** `ok` **prompt, use the** `printsmcenv` **command to display the configuration block.**

```
ok printsmcenv
config-version         : 1
backplane-type         : 0
reset-action           : 66
sir-xir-enable         : 2
back-end-power-option  : 0
chassis-type           : 0
flash-device           : 0
set-role-option        : 0
ipmi-checksum-ctlr     : 1
healthy-option         : 0
byteB                  : 0
byteC                  : 0
byteD                  : 0
byteE                  : 0
byteF                  : 0
byte10                 : 0
```

If `flash-device` is set to any other value besides 4, you will need to set it to 4 in order to exchange the system flash and user flash memory allocations.

2. **If the** `flash-device` **value is not equal to 4, use the** `setsmcenv` **command to set it to 4.**

```
ok setsmcenv flash-device 4
```

3. **Gracefully power-down the board and remove it from the chassis.**

4. **Locate the SW3 DIP Switch on the component side of the board.**

The SW3 DIP switch is located slightly under the heat-sink on the board. FIGURE 4-4 shows the location and default setting of the SW3 DIP switch.

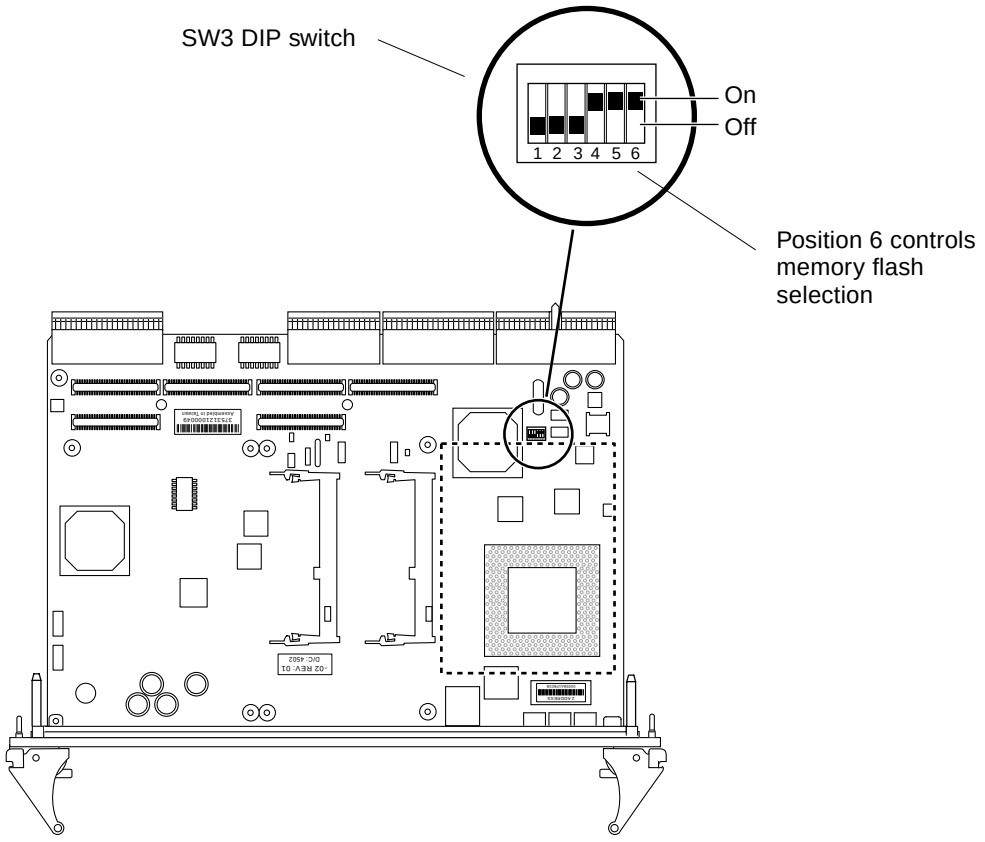

FIGURE 4-4 SW3 DIP Switch Location

SW3 DIP switch position 6 controls the flash memory selection. When position 6 is set to on (default), system flash will be assigned 1 MByte of memory and user flash will be assigned 7 MBytes of memory.

When SW3 DIP switch position 6 is set to off, and the `flash-device` setting of the configuration block is set to 4, user flash will be assigned 1 MByte of memory and system flash will be assigned 7 MBytes of memory.

Caution – Do not modify the settings on position 1 through 5 on the SW3 DIP switch. These positions are not user-selectable and any change to these positions' settings could critically damage the Netra CP2300 board.

5. **To set the flash memory selection, set the SW3 DIP switch position 6 to off.**

   See FIGURE 4-4 for the location of the SW3 DIP switch.

6. **Re-install the Netra CP2300 board into the chassis or system.**

   See Chapter 2 for installation instructions.

7. **Power on the Netra CP2300 board and display the OpenBoot PROM** `ok` **prompt.**

   After setting the DIP switch and the `flash-device` setting, the system flash will be assigned 7 MBytes of memory and the user flash will be assigned 1 MByte of memory (see FIGURE 4-5).

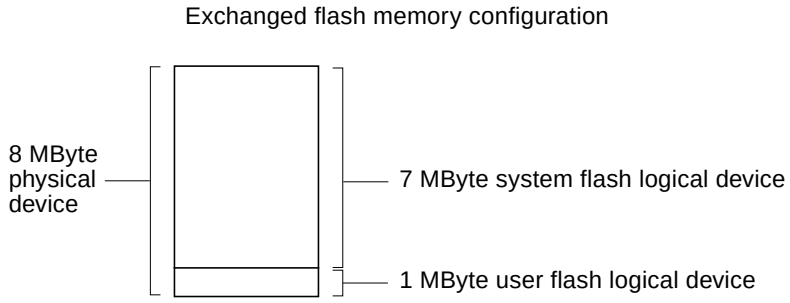

FIGURE 4-5 Exchanged System Flash and User Flash Logical Devices

4.7.2 Determining the Flash Memory Settings

If you are unsure if system flash is allocated the default 1 MByte of memory or 7 MBytes of memory, you can use the OpenBoot `devalias` command to see where user flash logical device begins.

Using the `devalias` command at the `ok` prompt, you can see where the user flash device path begins. By default, the system flash will use 1 MByte of space, so the user flash will begin at 100000 bytes (0 to fffff will be used by the system flash):

```
ok devalias uflash
uflash     /pci@1f,0/pci@1,1/isa@7/flashprom@1f,100000
```

If the SW3 DIP switch position 6 is set to off, and the `flash-device` is set to 4, the system flash uses 7 MBytes of space and the user flash device path will begin at 700000 (0 to 6fffff will be used by the system flash):

```
ok devalias uflash
uflash     /pci@1f,0/pci@1,1/isa@7/flashprom@1f,700000
```

In both situations, the system flash device path will start at 0, so you should not use it to determine the flash memory sizes:

```
ok devalias flash
flash     /pci@1f,0/pci@1,1/isa@7/flashprom@1f,0
```

4.7.3 Updating Flash Memory

Use the `flash-update` and `flat-update` OpenBoot PROM commands to update the flash memory on the Netra CP2300 board. Use the `flash-update` command to update the Netra CP2300 board's OpenBoot PROM or add OpenBoot PROM drop-in packages, and use the `flat-update` command to add any raw device to flash memory.

The command formats are:

`flash-update` *file-path flashtype*

`flat-update` *file-path flashtype*

Where *file-path* is the path to the flash update image, and *flashtype* can be:

- `systemprom`—updates the system flash
- `uflash`—updates the user flash

4.7.4 SMC Firmware Update

You can only update the SMC firmware at the OpenBoot PROM `ok` prompt.

To update the SMC firmware:

1. **Contact your Field Application Engineer to acquire the updated SMC firmware image.**
2. **Save the firmware to a directory on the system.**
3. **Use the `smc-flash-update` command to update the SMC firmware:**

```
ok smc-flash-update filename
```

Replace *filename* with the filename and full path to the SMC firmware image.

Note – *filename* must point to a valid SMC firmware binary image or the file cannot be read to complete the flash update.

4.8 Firmware Diagnostics

The firmware contains a comprehensive set of hardware diagnostic modules that provide tests for most situations. FIGURE 4-1 shows the control-flow relationship of the diagnostic modules with the system firmware. SunVTS can be executed from within the Solaris software if more tests are required. For more information, see Section 3.3, “Downloading and Installing SunVTS” on page 3-6.

The firmware diagnostic modules are:

- Basic POST (BPOST)
- Comprehensive POST (CPOST) – optional
- Extended POST (EPOST) – OEM supplied drop-in
- OBDiag

The firmware diagnostics cover address and data bits on all system buses and exercise the function of the major hardware resources on the board.

Diagnostics can be performed at OpenBoot PROM level by using the `obdiag` command, or by typing individual test commands at the `ok` prompt. These test suites are similar to those in earlier OpenBoot PROM versions but they are comprised of drop-ins that can be placed by the user. See the reference to the *OpenBoot 4.x Command Reference Manual* listed in Appendix D.

4.8.1 Setting Diagnostic Levels

The user interface for running POST at minimum or maximum remains the same. BPOST is embedded within firmware CORE and is executed when the OpenBoot PROM environment variable, `diag-switch?` is set to `true` and `diag-level` is set to `min`. Similarly, CPOST (and EPOST if it is present) is executed when `diag-level` is set to `max`. The permutations are shown in TABLE 4-4.

CPOST and Extended POST are clients of firmware CORE.

4.8.2 Basic POST (BPOST)

BPOST is integrated into firmware CORE. The first part of BPOST executes from flash memory. It is designed to validate enough of the system resources to be able to run firmware CORE in main memory (system RAM). If this test phase is passed, BPOST is also copied into system RAM. BPOST runs when the `diag-switch?` is set to `true` (see TABLE 4-4).

The part of BPOST executed from flash includes basic tests for the following:

- SRAM
- I-cache and D-cache
- MMU
- FPU
- L2-cache tag and RAM
- Data lines
- CORE memory

The second part of BPOST is performed after firmware CORE is copied into main RAM. This part of BASIC POST executed from RAM includes:

- Memory address line test – test assumes that the CPU, MMU, and FPU are functional.
- ECC block memory test – verifies main memory with block write and ECC checking. This test assumes that the CPU, MMU, and FPU are functional.

4.8.3 Comprehensive POST (CPOST)

Comprehensive POST (CPOST) is a client of firmware CORE. It is a dropin module invoked by firmware CORE and contains enhanced diagnostics for the CPU and on-board devices.

The execution of CPOST is optional and can be selectively controlled by an environment variable (see TABLE 4-4). CPOST runs after BPOST. To run CPOST, set the environment variables `diag-switch?` to `true` and `diag-level` set to `max`

CPOST tests include:

- Memory stress test; advanced main memory test
- Basic PBM, IOMMU test
- Basic Advanced PCI Bridge APB test
- Davicom Ethernet 1, 2
- South Bridge ISA, PMC, IDE, USB tests
- System Management Controller test

After CPOST the system undergoes a software reset which sends it back to firmware CORE. From this point, execution enters OpenBoot PROM (since diagnostics are only executed at power on reset).

4.8.4 OpenBoot PROM On-Board Diagnostics

The OpenBoot PROM on-board diagnostics reside in the OpenBoot PROM drop-in. These diagnostics are described fully in the *OpenBoot 4.x Command Reference Manual (*see Appendix D).

To execute the OpenBoot PROM on-board diagnostics, the system must be at the `ok` prompt. The OpenBoot PROM on-board diagnostics include:

- `watch-clock`
- `watch-net` and `watch-net-all`
- `probe-scsi`
- `test` *device path*
- `test-all`

4.8.5 OpenBoot Diagnostics

The OpenBoot Diagnostics are an enhancement of the traditional system tests. They reside in Forth script in a drop-in and are invoked with an interactive tool that is started from the `ok` prompt by typing **`obdiag`**.

When you start the OpenBoot Diagnostics, you should see the following menu:

```
ok obdiag
_____________________________________________________________________
|                              o b d i a g                            |
|_____________________________ _____________________________________|
|                           |                           |           |
|  1 ethernet@1             |  2 ethernet@2             |  3 flashprom@1f,0      |
|  4 flashprom@1f,100000    |  5 i2c-nvram@0,8e         |  6 ide@d               |
|  7 pmu@3                  |  8 serial@0,2e8           |  9 serial@0,3f8        |
| 10 usb@a                  |                           |                        |
|___________________________|___________________________|________________________|
|   Commands: test test-all except help what printenvs setenv versions exit  |
|____________________________________________________________________________|
```

At the obdiag prompt, type test-all to display a printout similar to the following:

```
obdiag> test-all
Hit the spacebar to interrupt testing
Testing /pci@1f,0/pci@1,1/ethernet@1 ................................ passed
Testing /pci@1f,0/pci@1,1/ethernet@2 ................................ passed
Testing /pci@1f,0/pci@1,1/isa@7/flashprom@1f,0 ...................... passed
Testing /pci@1f,0/pci@1,1/isa@7/flashprom@1f,100000 ................. passed
Testing /pci@1f,0/pci@1,1/pmu@3/i2c@0,0/i2c-nvram@0,8e .............. passed
Testing /pci@1f,0/pci@1,1/ide@d ..................................... passed
Testing /pci@1f,0/pci@1,1/pmu@3 ..................................... passed
Testing /pci@1f,0/pci@1,1/isa@7/serial@0,2e8 ........................ passed
Testing /pci@1f,0/pci@1,1/isa@7/serial@0,3f8 [Used as Console] ........ passed
Testing /pci@1f,0/pci@1,1/usb@a ..................................... passed

Hit any key to return to the main menu
```

CHAPTER 5

Hardware and Functional Description

This chapter contains the following sections:

5.1 Summarized Physical Description

The Netra CP2300 board is a 6U-sized cPSB circuit card with CompactPCI connectors J1 (labeled as J9 on the board) and J2 (J10) for PCI, and J3 (J13) and J5 (J14) for I/O. The CompactPCI J4 connector is not fitted to the board. See FIGURE 5-1 and FIGURE 5-2 for top and solder-side views of the board.

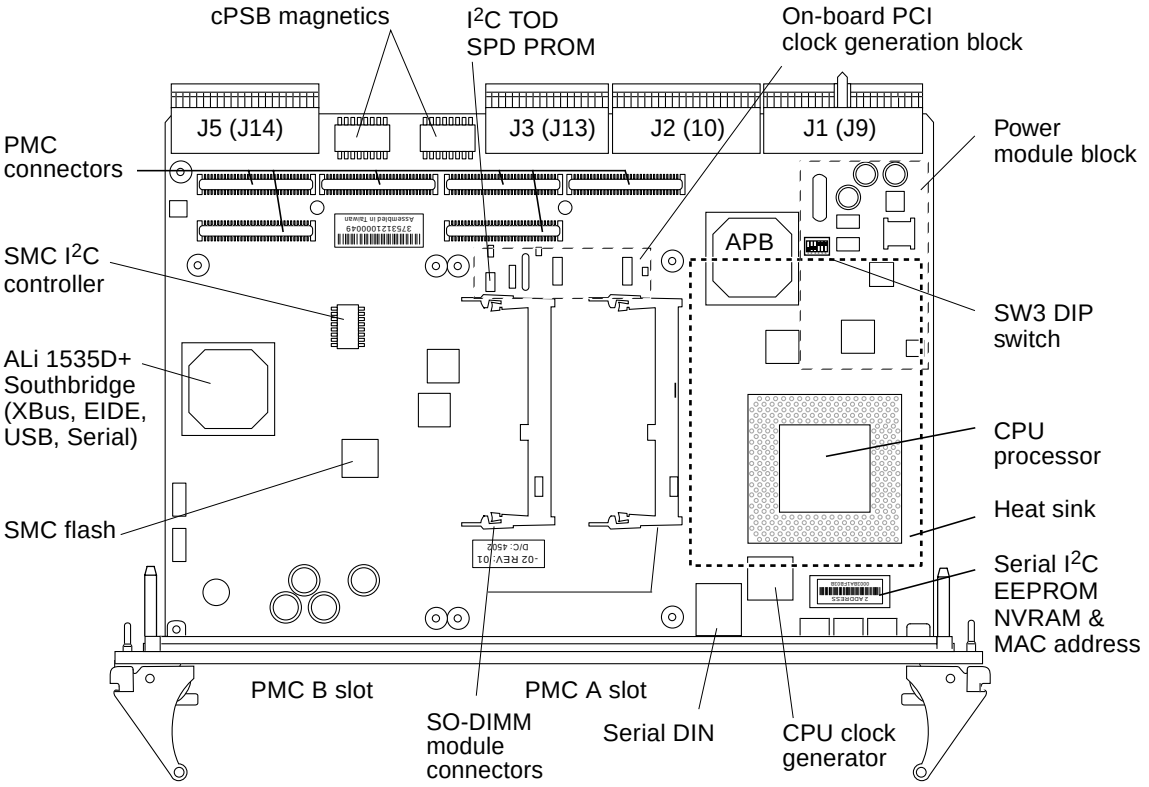

FIGURE 5-1 Netra CP2300 Board Layout

Note – The heat sink is shown as dotted lines in this diagram to illustrate the components on the board that lie beneath these devices.

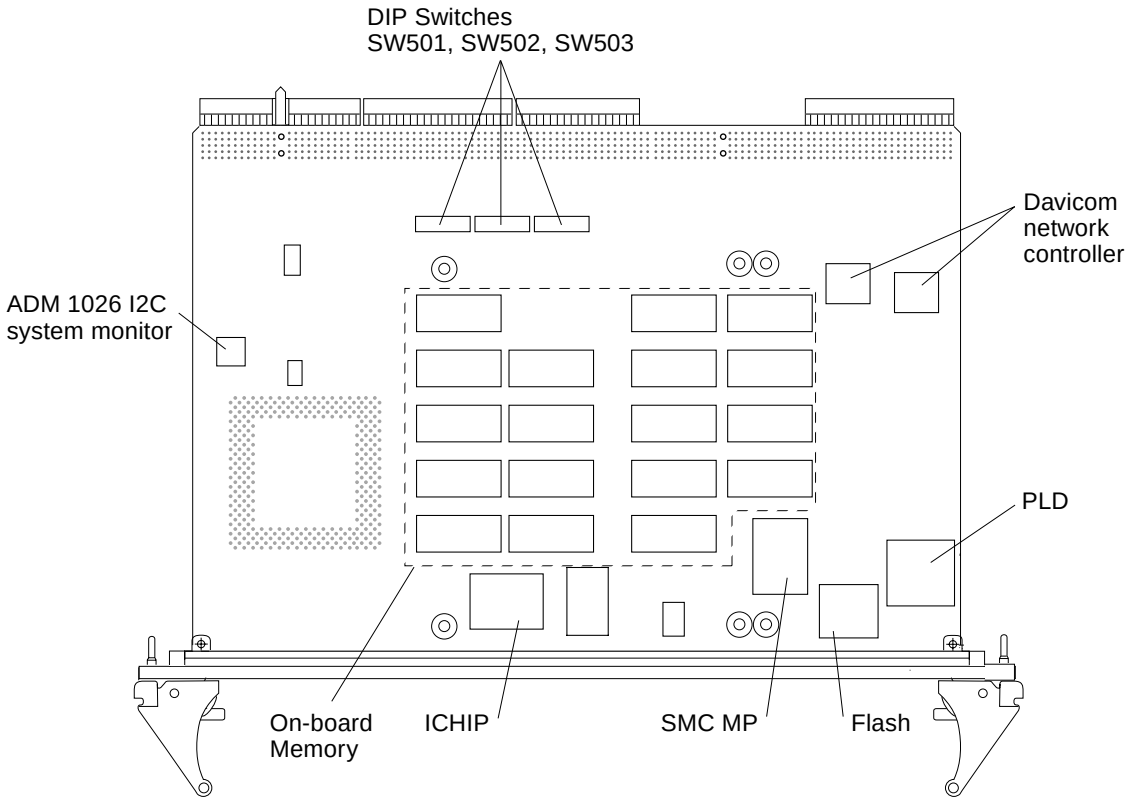

FIGURE 5-2 Typical Netra CP2300 Board – Solder Side

The Netra CP2300 board functions as a cPSB node board. The board has the following I/O access:

- One serial port on the front panel.
- Through the backplane: a transition card must be connected to provide rear connector access for two serial ports, two optional switch-selectable Ethernet ports, a switch-selectable EIDE connector, and a USB port. Sun Microsystems offers a compatible Netra CP2300 cPSB transition card (part number, XCP2300-TRN, 375-3134-*xx*). This card is recommended for use with the Netra CP2300 board, but OEM developers may design their own transition card instead.
- Two PMC card interfaces can accept two PMC I/O cards.
- The Netra CP2300 transition card has two PIM interfaces that can accept two PIM cards that can bring the PMC ports out to its panel at the rear of the enclosure. See Section 5.4.2, “PMC and PIM Interface” on page 5-12 for further details.

The front panel of the Netra CP2300 board has two PMC module slots, a serial port, and the following status LEDs:

- ABORT – push button (XIR)
- RESET – push button (POR)
- USER – yellow
- READY – green
- Blue LED for hot-swap

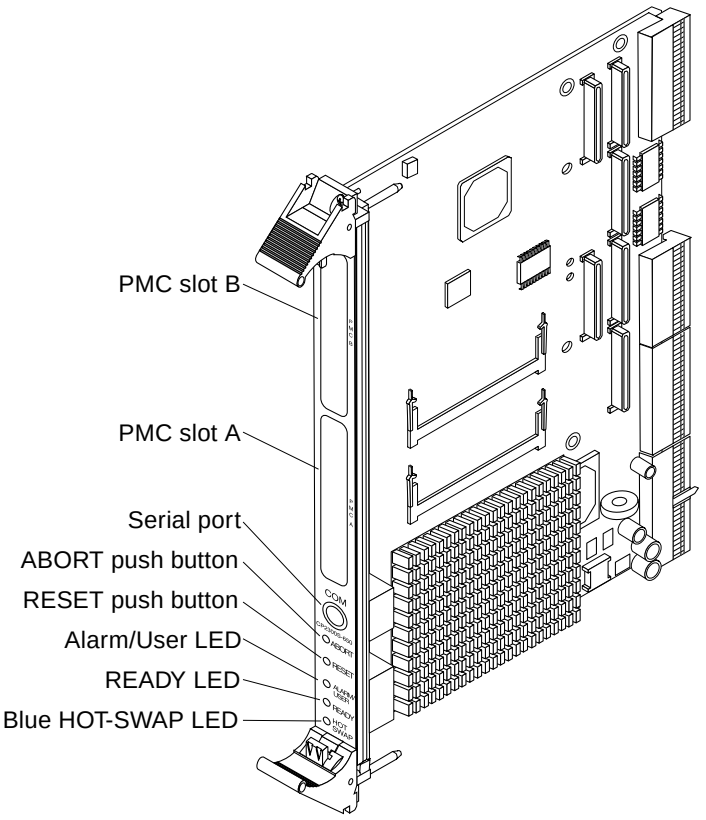

FIGURE 5-3 Front Panel of a Typical Netra CP2300 Board Assembly With Heat Sink

5.2 Detailed Description

A simplified schematic diagram is shown in FIGURE 5-4.

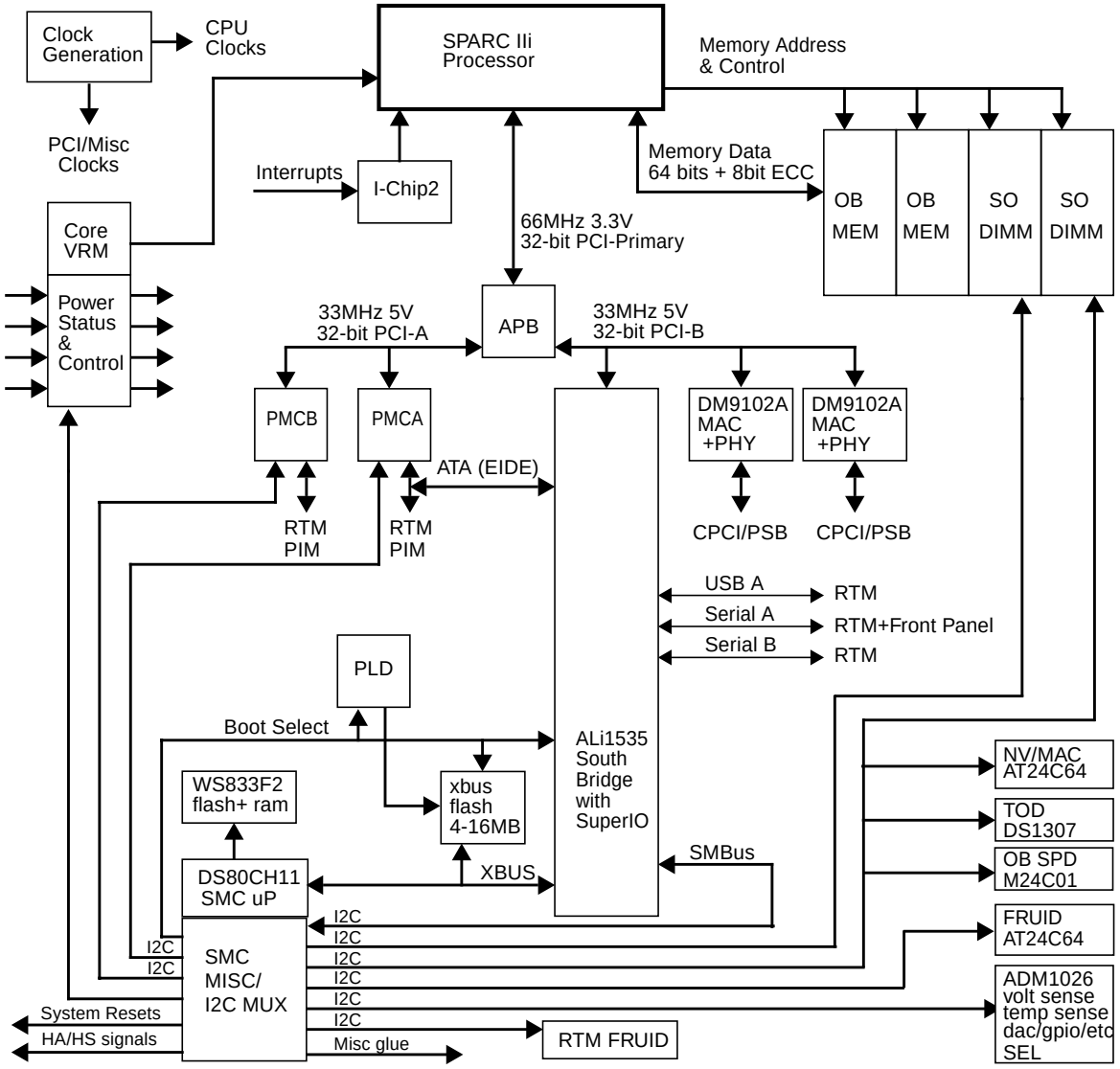

FIGURE 5-4 Netra CP2300 Board Functional Block Diagram

The L2-cache is integrated into the UltraSPARC IIi processor package. This processor is supported by SDRAM memory that is soldered onto the board and is also available in plug-in module form.

Apart from incoming interrupts, the processor handles all I/O through its built-in 66 MHz, 32-bit PCI bus interface. This interface is used to connect to a Sun Advanced PCI Bridge (APB) that services two 33 MHz 32-bit downstream interfaces, PCI bus A and PCI bus B.

PCI Bus B connects the APB to two Davicom Ethernet packages and the South Bridge. In addition, The PCI bus A from the APB connects to each of two 33 MHz, 32-bit PMC interfaces on the host board. See Section 5.4.2, “PMC and PIM Interface” on page 5-12 for more details.

The SMC connects to:

- The on-board I^2C bus, enabling it to communicate with sensors and controls.
- The User IPMI bus, enabling user management of other entities in the system. Peripheral hot-swap control is also enabled through this path.
- The power subsystem.

The SMC controls the startup of the board, because it activates the power module and controls the system reset signals. In addition, it handles hot-swap signals from the CompactPCI backplane, for example: HEALTHY and BD_SEL. See Section 1.3, “Hot-Swap Support” on page 1-9 for more information on hot-swap.

5.3 CPU and Main Memory Subsystems

This section describes the UltraSPARC IIi processor and additional memory on the Netra CP2300s. FIGURE 5-5 shows the UltraSPARC IIi interfaces.

5.3.1 UltraSPARC IIi Processor

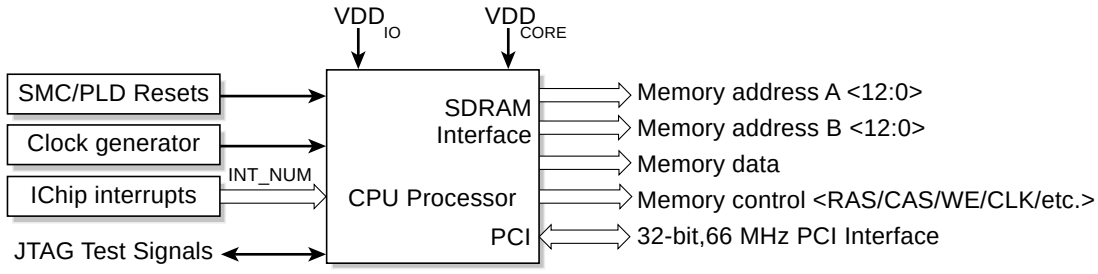

FIGURE 5-5 UltraSPARC IIi Interface

The Netra CP2300 board uses the UltraSPARC IIi 650 MHz processor. The processor is housed in a 370-pin ceramic pin grid array (PGA) package. It typically dissipates no more than 18 W at 650 Mhz (the entire Netra CP2300 board may dissipate 25 W).

The UltraSPARC IIi processor is directly connected to the board SDRAM through a 72-bit (64-bit DATA plus 8-bit ECC) path. Dual address buses reduce capacitive loading and increase the memory density beyond that of unbuffered devices.

The CPU connects to the APB by means of a 32-bit, 66 MHz PCI interface which the APB in turn translates to two downstream 33 MHz PCI buses.

The UltraSPARC processor begins execution from a fixed image in a PROM that lies on the XBus. The processor accesses this XBus in a boot path that automatically includes the APB, 1535 Bridge, and XBus.

Processor resets are received from the system management controller (SMC). See Section 5.7, “Resets” on page 5-24 and FIGURE 5-16 for more details.

The various interrupts on the board are encoded by the I-chip2 to appear at the UltraSPARC IIi processor as 6-bit parallel data. See Section 5.7, “Resets” on page 5-24 for more information.

The processor I/O is run at a fixed VDDIO of 3.3V but the core voltage, VDDCORE, is adjustable and configured according to CPU type, typically in the range of 1.3 V to 1.9 V.

JTAG / Test signals are available for use in boundary scan diagnostics.

5.3.2 Memory Address Mapping

The UltraSPARC IIi L2 cache megacell reserves a 4 GB region for cacheable main memory. The memory databus width and the module databus width are of equal size (64-bit data plus 8 bit ECC) so memory modules can be installed in mixed sizes.

The UltraSPARC IIi Address Data Generation Logic (ADGL) logically maps modules according to their size, rather than their physical location. The largest sizes are mapped to the lowest address ranges. Where modules of identical size are present, the lower slot number is mapped to the lower address range.

FIGURE 5-6 shows a memory mapping example.

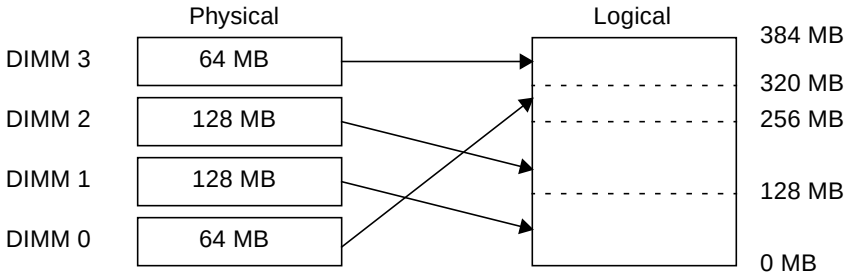

FIGURE 5-6 Memory Mapping Example

5.3.3 SDRAM Memory

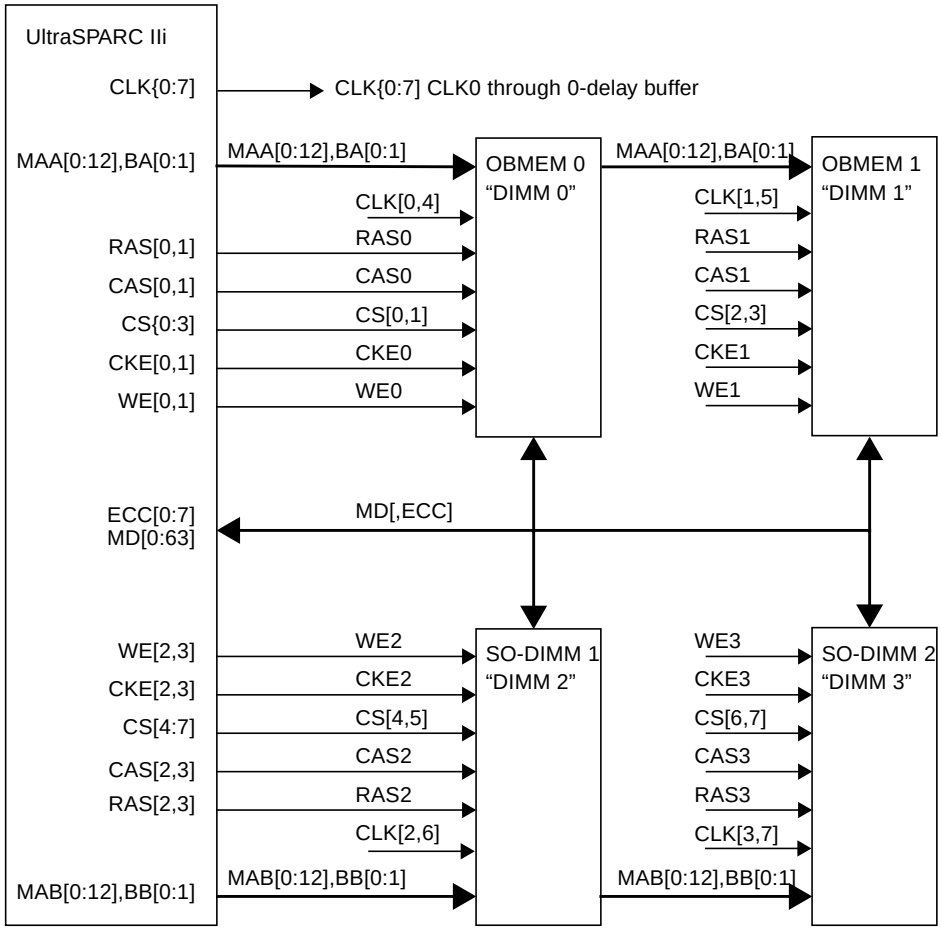

FIGURE 5-7 SDRAM Memory Interface

The UltraSPARC IIi 650 MHz processor connects directly to the memory with a 72-bit (64-bit DATA plus 8-bit ECC) data bus. The memory can be either on-board SDRAM only or can include additional SO-DIMM memory modules.

Each module is equipped with a serial EEPROM device containing 256 bytes of presence detect data.

The memory block, whether on-board or a module, provides non-volatile serial memory to enable the Serial Presence Detect function. This memory can be interrogated by the SMC through the I^2C interface.

5.3.4 Memory Components

This section describes additional memory available on the Netra CP2300 boards.

5.3.4.1 System (Boot) Flash Memory

The system flash usually resides in 1 Mbyte of space (see Section 4.7.1, “Exchanging the System and User Flash Memory Devices” on page 4-20 for more information). It contains Common Operations and Reset Environment (CORE) firmware, Comprehensive POST, and OpenBoot PROM boot code. The system flash may be upgraded by running a program out of OpenBoot PROM or executing a Solaris software script. If the system flash becomes corrupted, contact your nearest Field Application Engineer.

5.3.4.2 User Flash Memory

The board is usually equipped with 7 Mbyte of user flash memory (see Section 4.7.1, “Exchanging the System and User Flash Memory Devices” on page 4-20 for more information). You may use the flash memory for various purposes such as storage for RTOS, user data storage, OpenBoot PROM information, or to house drop-ins. Drop-ins simplify customizing a system for the user.

A DIP switch SW503 and an SMC configuration block setting determines whether the user flash is bootable during OpenBoot PROM boot and whether it is write enabled (see Section B.5, “DIP Switch Settings” on page B-20).

5.3.4.3 NVRAM

The Netra CP2300 board uses the I^2C serial EEPROM to save configuration variables.

These boards uses a time-of-day (TOD) I^2C device and a 8 Kbyte serial EEPROM. These components provide:

- A time-of-day (TOD) real-time clock, which features 56 bytes of non-volatile SRAM. The real-time clock counts seconds, minutes, hours, day the of month, month, day of week and year, with leap year compensation. Address and data are transferred serially through the 2-wire bi-directional bus.
- 8 Kbyte storage for environment variables, user modifiable. The Ethernet address and Host ID are stored in the system flash. These values are copied to the I2C SEEPROM when the system is powered-on.

5.3.4.4 Serial I^2C EEPROM

This device stores the OpenBoot PROM configuration variable settings, the board MAC address, and the Host ID in a removable serial EEPROM that is accessible through the I^2C bus.

5.3.4.5 FRU ID I^2C EEPROM

The FRU ID I^2C EEPROM chip stores manufacturing-related information of the Netra CP2300 board. This information is useful only when the Netra board is being serviced.

See Appendix C for details on accessing the FRU ID information for the board.

5.4 Bus Subsystems

There are three internal PCI buses on the board. One of the internal PCI buses, PCI bus B, is bridged to the slower ISA-speed XBus.

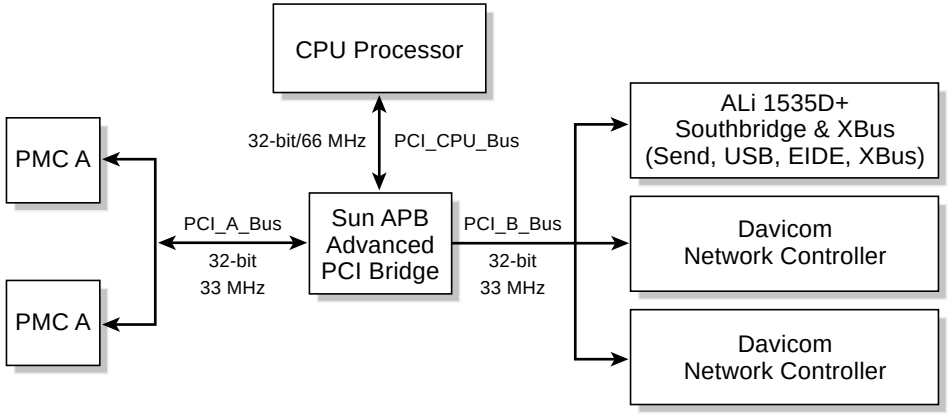

FIGURE 5-8 Netra CP2300 PCI Bus Interface, 33MHz CompactPCI Bridge

5.4.1 APB PCI Bus Interfaces

The UltraSPARC IIi CPU has an integrated 32-bit/66 MHz PCI bus interface. The Advanced PCI Bridge—acting as a North Bridge—splits this bus into two 32-bit/33 MHz PCI buses. Of these, the PCI A bus connects to the PMC slots and the PCI B bus connects to the onboard I/O devices.

5.4.2 PMC and PIM Interface

The PCI mezzanine card (PMC) interface is defined by IEEE and PICMG standards:

- IEEE P1386, presently in draft form, defines the Common Mezzanine Card (CMC) mechanical profile (*common* because this definition, for example, can also apply to a VME rendering)
- P1386.1 defines the PCI electrical interface through its connectors Pn1/Jn1 through Pn4/Jn4
- PICMG 2.3 R1.0, *PMC on CompactPCI Specification* maps the PMC signals from the Jn1 through Jn4 connectors on the CompactPCI board through the CompactPCI backplane connections. In the case of the Netra CP2300 board, these connections are routed to the CompactPCI J3 (labeled as J13 on the board) and the J5 (J14) connectors.

The PMC interface enables you to use Independent Hardware Vendor (IHV) PMCs to implement additional I/O from the host at the system integration level.

The Netra CP2300 cPSB transition card provides two slots for PIM cards. A PIM card enables rear I/O functions when paired with a PMC card installed on the front panel of the board.

A PIM must have a corresponding PMC in the front slot because the PMC board performs an adapter function between the PCI bus A and the user I/O signals passed through a CompactPCI backplane connector to the PIM slot on the transition card. When a PMC that has a front-panel connector is used with a PIM, jumpers are typically set to disable its front I/O operation.

FIGURE 5-9 illustrates the interconnection between PMC and PIM slots for installed PIMs. The numbers in parentheses show how the connectors are labeled on the Netra CP2300 node board and transition card.

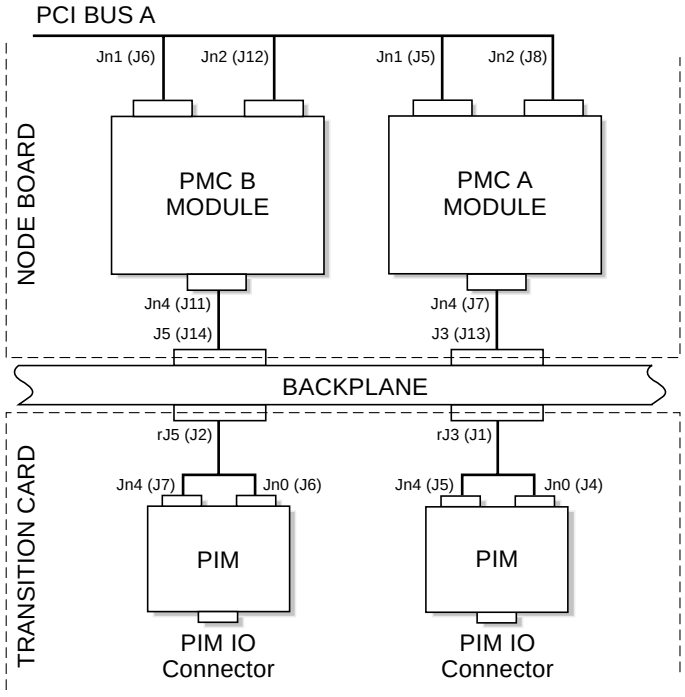

FIGURE 5-9 PIM Installation Configuration

FIGURE 5-10 shows the PMC B connectors and card attachment to a Netra CP2300 board. There is a second PMC slot, PMC A, adjacent to the first (see FIGURE 5-11).

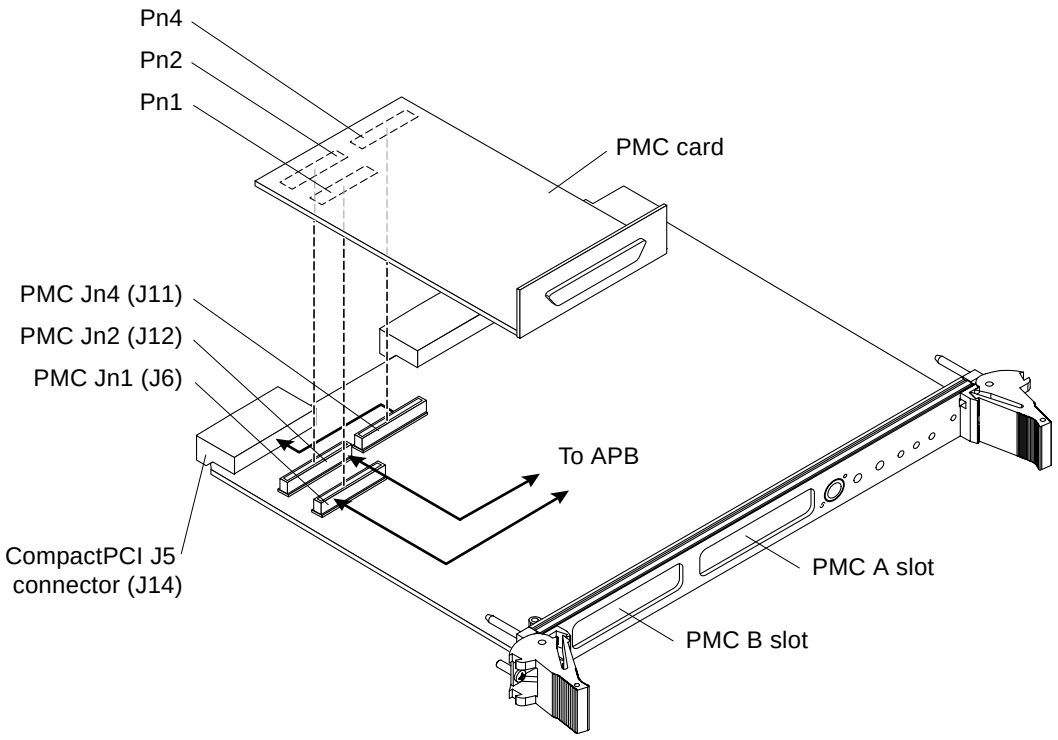

FIGURE 5-10 Data Paths in PCI Mezzanine Module Interface on Host Board

For the PMC B slot, the APB on the Netra CP2300 board supplies PCI bus signals to PMC B connectors Jn1 (labeled as J6 on the board) and Jn2 (J12). The PMC card logic decodes its specific I/O interface, which it makes available at the front panel.

The 64-pin PMC Jn3 connectors are not fitted to the Netra CP2300 board. These connectors are specified for expansion for 64-bit PCI (it carries the upper 32 bits), which is not provided. A 64-bit capable PMC card can function in these slots but its bus interface is constrained to 32 bits.

The PMC B Jn4 (J11) connector is specified for user I/O and carries PMC signals to the CompactPCI J5 (J14) backplane connector. If a transition card is installed, this CompactPCI J5 (J14) connector I/O is conditioned by an IHV-supplied PIM card to provide the matching I/O on the enclosure back panel. Its backplane I/O is routed to the CompactPCI J5 (J14) connector.

In the case of the PMC A slot on the Netra CP2300 board, the PMC A Jn1 (J5) and the PMC A Jn2 (J8) connectors are similarly attached to the APB, but the user I/O from the PMC A Jn4 (J7) connector is routed out of CompactPCI J3 (J13) backplane connector.

See FIGURE 5-11, TABLE 5-1, and TABLE 5-2 for more information about the Netra CP2300 board PMC and CompactPCI backplane connector labelling.

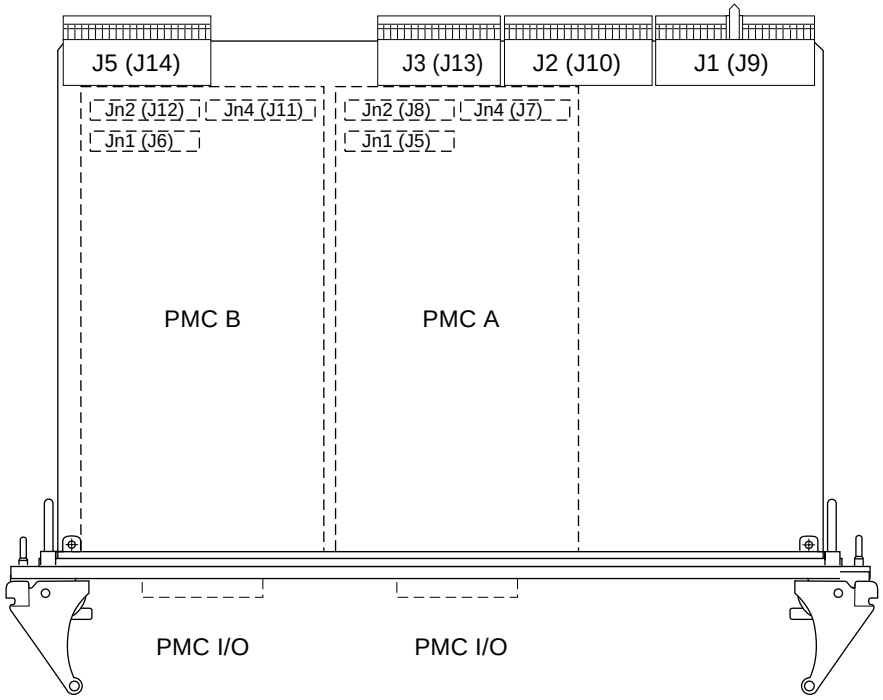

FIGURE 5-11 PMC Connector Interfaces on the Netra CP2300 Board

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Note – The P1386.1 standard reserves the Jn3 64-pin connector for PCI 64-bit extensions, so it is not fitted on the Netra CP2300 board.

TABLE 5-1 lists how the PMC slot connectors are labeled on the board, and TABLE 5-2 lists how the CompactPCI backplane connectors are labeled.

TABLE 5-1 PMC Connector Labelling

PMC Slot	PMC Connector	On-Board Connector Label
PMC slot B	Jn1	J6
PMC slot B	Jn2	J12
PMC slot B	Jn3	Not fitted
PMC slot B	Jn4	J11
PMC slot A	Jn1	J5
PMC slot A	Jn2	J8
PMC slot A	Jn3	Not fitted
PMC slot A	Jn4	J7

TABLE 5-2 CompactPCI Backplane Connector Labelling

CompactPCI Backplane Connector	On-Board Connector Label
J1	J9
J2	J10
J3	J13
J4	Not fitted
J5	J14

5.4.3 I^2C and IPMI Channels

The SPARC domain I^2C controller is located on the ALi 1535D+ South Bridge chip. The SMC also has two on-board I^2C channels used for IPMI and one external I^2C controller to access on-board I^2C devices.

I^2C communication is used:

- To implement the IPMI interface for system management.
- To provide a means of performing local environmental monitoring which tracks—and controls where appropriate—local board or chassis “housekeeping” functions. These functions include: monitoring of temperature, FRU ID, MAC address, and memory type and size.
- To provide an interface for user monitoring and control, for example chassis temperature or fan operation.

The I^2C paths are shown in FIGURE 5-12.

Each I^2C device on the board uses common addressing pins. The devices are distinguished by the internal device ID and selectable address pins. All I^2C devices are supplied from IPMB or early power before backend power is established whenever possible (see Section 5.8, “Power Subsystem” on page 5-26 for further details).

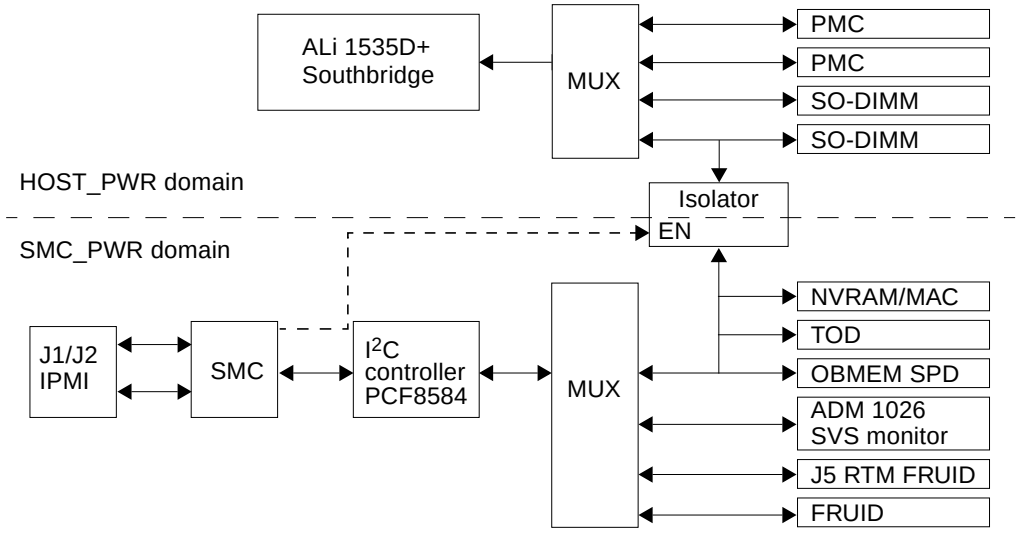

FIGURE 5-12 Netra CP2300 Board I^2C and SMBus Architecture

5.5 System Input/Output

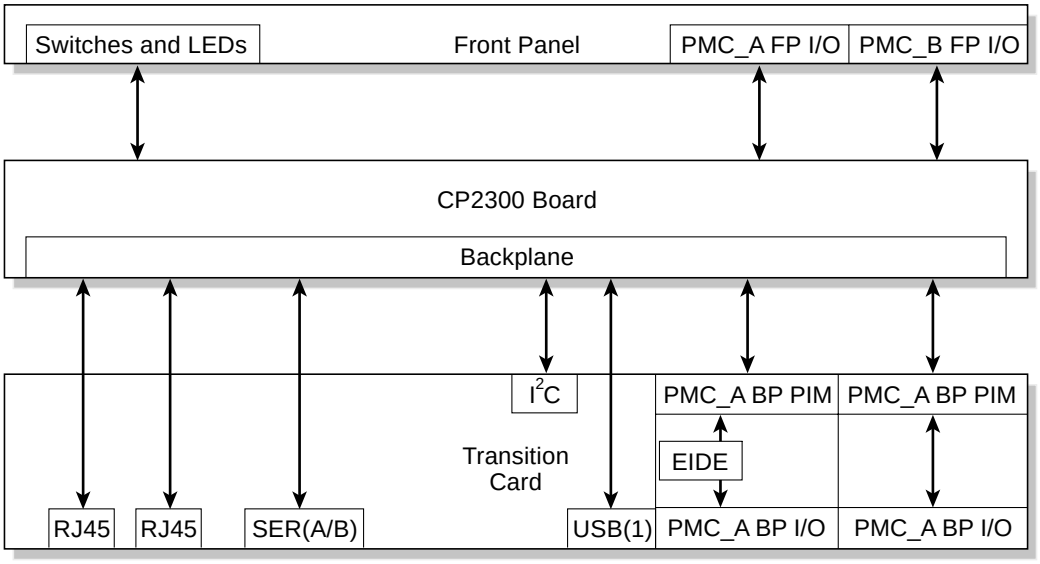

FIGURE 5-13 Netra CP2300 Board and Transition Card I/O Interfaces

FIGURE 5-13 shows the I/O for the Netra CP2300 board. The I/O functions can be categorized into four groups which are described in the following sections.

5.5.1 Front-Panel I/O

FIGURE 5-14 illustrates the indicators and I/O connectors on the Netra CP2300 front panel. The Netra CP2300 front panel connectors, buttons and LEDs are described below:

- Two peripheral mezzanine card (PMC) I/O bezels
- A serial connector (DIN8) which is also connected to serial port A of the 16552 UART on the board
- ABORT – An abort push button; passes an XIR signal to the SMC
- RESET – A reset push button; passes an Power-on-Reset (POR) signal to the SMC

- USER – A yellow LED that is defined by the user. The default function for the LED is to signal that the board is at an OK status. The colors are controlled by SPARC by way of the SMC. See the *Netra CP2300 cPSB Board Programming Guide* (817-1331-*xx*) for information on programming the user LED. You can download this document at:

`http://www.sun.com/products-n-solutions/hardware/docs/CPU_Boards/`

- READY – A green power LED, sourced from the power module and controlled by the SMC.
- A blue LED for hot-swap status, sourced from the SMC.

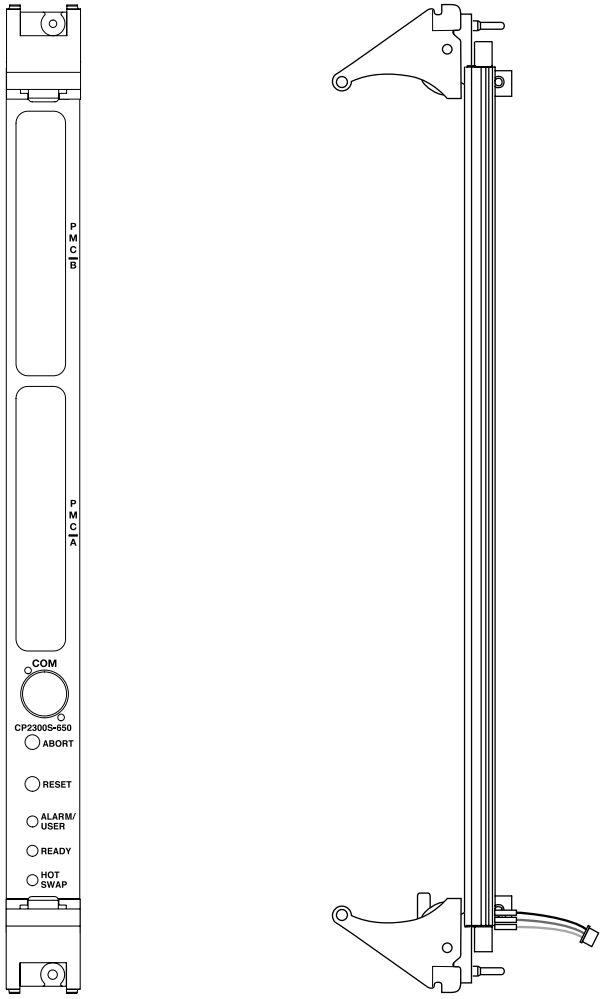

FIGURE 5-14 Netra CP2300 Board Front Panel

5.5.2 PMC Interface

The host board includes two PMC front-panel I/O cutouts to enable attachment of up to two PMC expansion cards. When installed, these cards access a PCI bus through compatible connectors provided on the host board. See “PMC and PIM Interface” on page 5-12.

5.5.3 Backplane I/O

Most of the I/O channels to or from the board are passed to the CompactPCI connectors: J3 and J5 (which are labeled J13 and J14 respectively). These channels are accessible from external connections on a transition card connected at the rear of the backplane. The CompactPCI J4 connector is not populated on these host boards to prevent contention with H110-compliant backplane signals. Contact assignments for these connectors are shown in Section B.4, “Backplane Connectors” on page B-12. For location of the connectors, see FIGURE 5-1.

5.5.3.1 CompactPCI J3 (J13) Signals

The user-defined PMC A I/O signals on the Netra CP2300 cPSB board provides matching I/O interfaces on the enclosure backpanel through the PIM cards installed on the Netra CP2300 transition card. The PMC A I/O signals are routed through board’s CompactPCI J3 connector (labeled as J13 on the board) to the transition card’s CompactPCI rJ3 connector (labeled J1 on the transition card).

5.5.3.2 CompactPCI J5 (J14) Signals

The following signal sets pass through the CompactPCI J5 backplane connector (labeled as J14 on the board) to connect to an external interface connector on the transition card:

- Two TP Ethernet channels from the PHYs
- Two serial channels
- A USB channel
- An I^2C channel
- PMC B I/O

The PMC B I/O signals are routed through board’s CompactPCI J5 connector (labeled as J14 on the board) to the transition card’s CompactPCI rJ5 connector (labeled J2 on the transition card).

5.6 System Management Controller

The System Management Controller (SMC) subsystem is one of the most important components of the system board. This subsystem provides a variety of service functions related to assuring availability of the system. These functions contrast with the board functions that execute applications.

The SMC consists of a small microcontroller with an SRAM for a software stack and nonvolatile memory for program storage and data logging. The SMC is modular in character, but is physically embedded into the circuitry of the Netra CP2300 board. FIGURE 5-15 shows its functional relationship with the system.

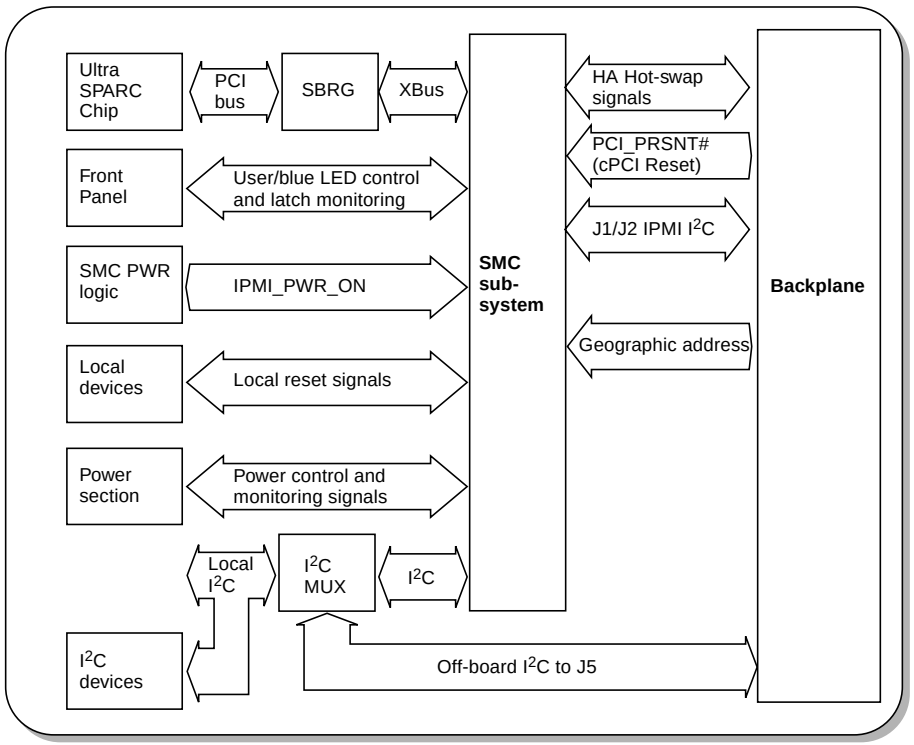

FIGURE 5-15 System Management Controller Interface

The SMC hardware and firmware implements the functions of system management and hot-swap control.

Note – Although the hardware and firmware functions are architecturally separate, reference to the SMC subsystem in this document—whose description is hardware oriented—refers to both functions.

The SMC controls the on-board CompactPCI interface for the hot-swap process.

In performing these functions, the design maintains conformance with the PICMG CompactPCI core specification and the PICMG CompactPCI hot-swap specification: See Appendix D for references to these documents. The main features that are supported by the SMC subsystem are:

- Coordinates and controls local resets on the system board during power-on reset, watchdog timeout, software initiated reset, and as a result of user intervention such as pushbutton reset or backplane reset.
- Supports a command and communications interface between the UltraSPARC IIi host processor and the SMC microcontroller by means of an interconnecting XBus. This interface accommodates a command suite from the UltraSPARC processor to the SMC and supports bidirectional interrupts between the UltraSPARC processor and the SMC.
- The board responds to the CompactPCI RST, HEALTHY, and BD_SEL signals from the active system controller (provided that this host provides HA hot-swap functions through the CompactPCI bus).

Note – This board does not provide HA hot-swap control for peripherals.

- Implements a two-level watchdog timer for the SMC processor and for the host processor.
- Supports three I^2C ports. One of the I^2C ports carries an IPMI bus that is routed through CompactPCI J1 backplane connector (labeled as J9) to enable communication with other SMCs in the system. The second I2C port carries IPMI signals to the CompactPCI J2 connector (J10). The third I^2C port serves a multiplexer that splits its input into four channels:
  - One channel provides communication with the FRU ID and motherboard (for example, temperature or FRU information)
  - A second channel is for user functions and transition card FRU ID and is passed to the CompactPCI J5 connector (J14)
  - A third channel is for ADM 1026 system monitoring
  - A four channel is for time-of-day (TOD), SPD, and other on-board devices
- Communicates with the system controller using the IPMI protocol over a backplane link, in accordance with the PICMG CompactPCI hot-swap specification. The SMC responds to commands from the active Baseboard Management Controller (BMC) when the host board is installed in a peripheral slot.

- Enables local a local environmental monitoring management scheme that monitors—and controls where appropriate—local board or chassis "housekeeping" functions through the on-board I^2C interface. Such functions include (see also Section 4.5, "Environmental Monitoring Support at OpenBoot PROM" on page 4-14):
  - Temperature sensing
  - Power supply voltage sensing
  - Power supply module on/off control
  - Memory module and on-board SPD detection
- Supports flash update – the SMC firmware supports external update of its flash PROM (see Chapter 4).
- Acts as a peripheral management interface, which includes:
  - IPMI communications with Baseboard Management Controller
  - Handling of hot-swap (HEALTHY/BD_SEL) related signals
  - Receiving system and CompactPCI reset events to generate local board reset

For full details on SMC and reset information, refer to Chapter 4.

5.6.1 Watchdog Timer

In the Netra CP2300 board, the SMC implements a two-level watchdog timer. The host-SMC command interface defines communication between host and SMC. The host and the SMC constantly communicate with each other when the watchdog timer is enabled. The SMC monitors the heartbeat of the CPU processor host. The heartbeat is sent in the form of a reset watchdog timer that is sent from the CPU to the SMC. The watchdog timer must be programmed to ensure that it does not get too close to the expiration. There should be some time accounted for the latency overhead or any unexpected event that may delay transmission of the heartbeat. For full details on programming the watchdog timer, refer to the *Netra CP2300 cPSB Board Programming Guide* (817-1331-*xx*).

The two levels of the watchdog timer are as follows:

- Countdown register timer (16 bits, 100 msec. resolution)
- Pre-timeout timer (1 sec. resolution)

The pre-timeout timer can only start if the countdown register timer has expired or has been set to zero. The two timers cannot run simultaneously.

The two watchdog timers are enabled by messages sent over the host-SMC command interface using the set watchdog timer command. The commands to enable the host-SMC command interface for watchdog timer functionality are:

- `smc-reset-wdt`
- `smc-set-wdt`
- `smc-get-wdt`

The uses of these functions are shown in TABLE 5-3.

TABLE 5-3 Host-SMC Commands for Watchdog Timer

Host-SMC Command	Uses
`smc-reset-wdt`	Starts and restarts watchdog timer from the initial countdown value
`smc-set-wdt`	Initializes, configures and stops the watchdog timer
`smc-set-wdt`	Retrieves current settings and present timer value of watchdog timer

5.7 Resets

This section provides details on resets for the Netra CP2300 board.

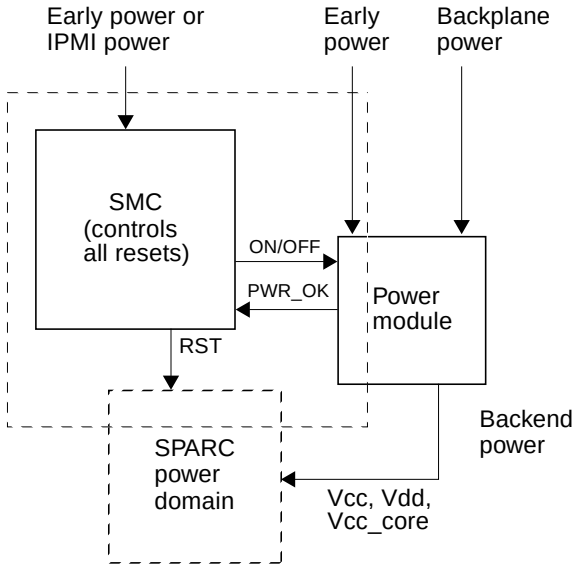

FIGURE 5-16 Simplified Reset Paths

Parts of the board are powered by *early power* before the SPARC domain receives power (backend power). For more information, see Section 5.8, “Power Subsystem” on page 5-26.

The SMC receives its power through the 5 volt standby (IPMI) power. However, if early power is present, the SMC switches itself to receive power from early power.

Once the SMC is out of reset and initialized, the SMC powers the CPU SPARC by turning on the backend power (power module). After the power module successfully powers-on, it will assert a POWER_OK signal. When the POWER_OK signal is asserted, the SMC will remove the CPU SPARC resets, which will allow the CPU to boot.

Note that:

- When the SMC is reset, the whole system is reset.
- When the CPU is reset, the CPU I/O is reset.

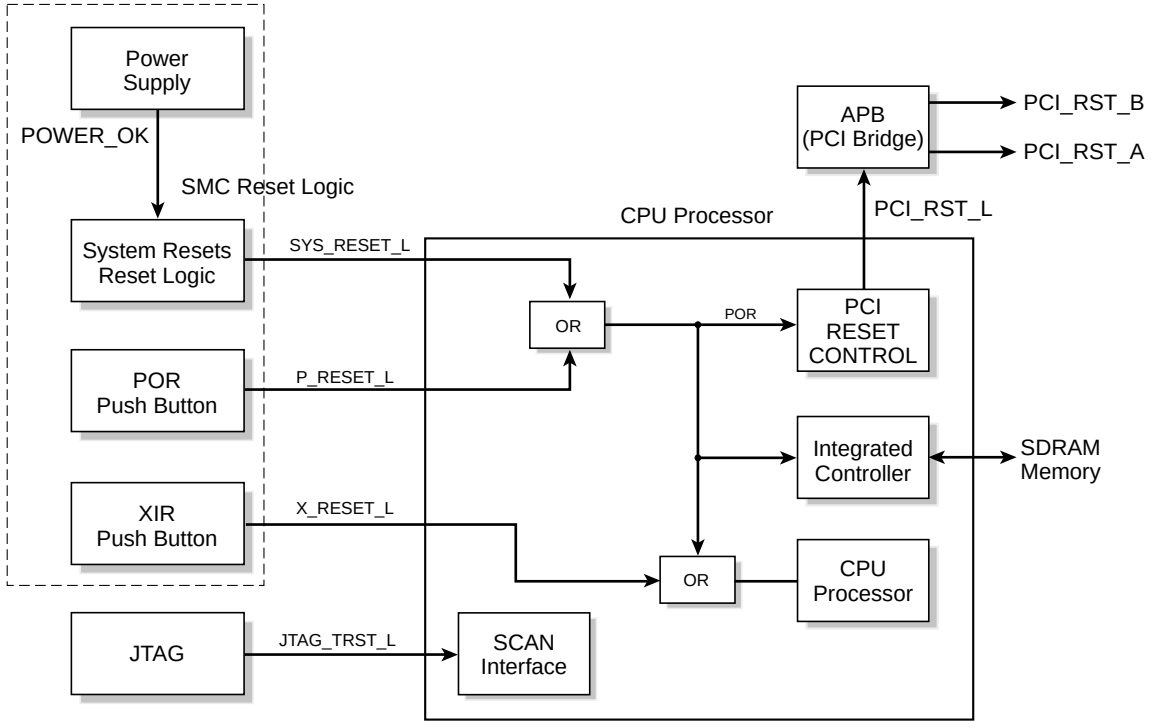

FIGURE 5-17 Simplified CPU Subsystem Reset Architecture

5.8 Power Subsystem

FIGURE 5-18 shows a simplified schematic diagram of the power subsystem. This subsystem can power the board to support a hot-swap environment.

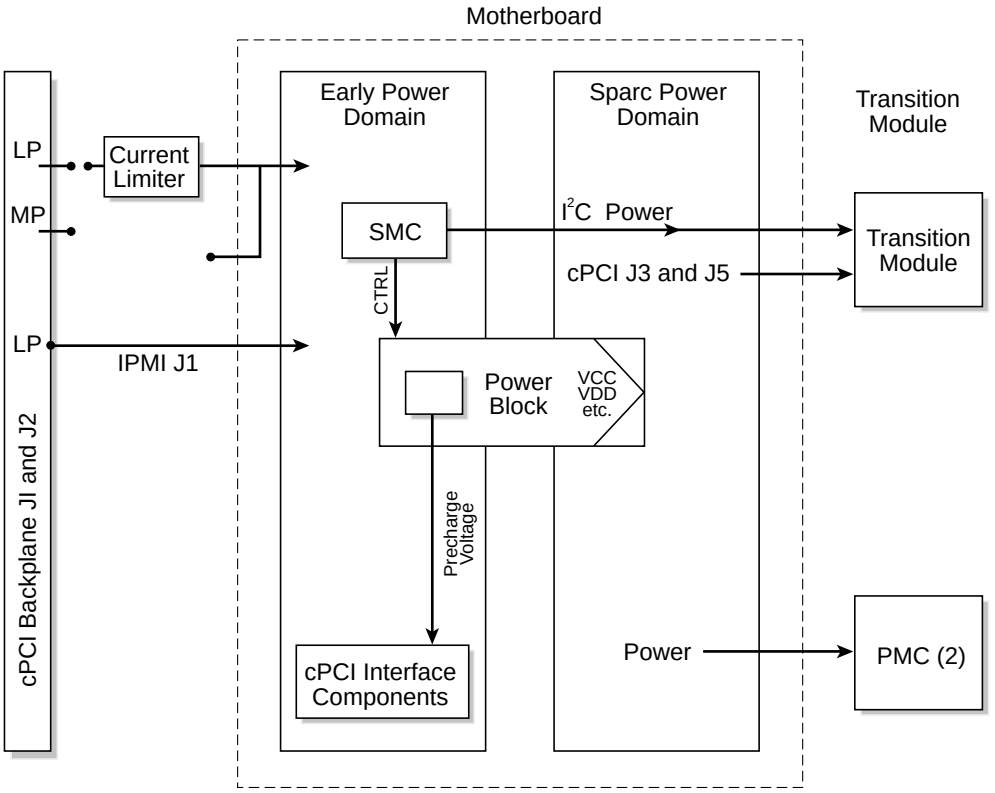

FIGURE 5-18 Power Distribution Block Diagram

Note – In FIGURE 5-18 I^2C power is derived from IPMI/early power.

The Netra CP2300 board sequences power in two time-separated domains:

- Early Power domain
- SPARC Power domain—this is the *Backend Power* in the PICMG hot-swap specification.

Early power is applied to the board from backplane long pins (LP in the figure) as the board is inserted. Early power current flows to board subsystems:

- Power block – supplies precharge current to the CompactPCI bus interface components.
- SMC – needed to control logical state of the CompactPCI interface circuits as they are connected.
- IPMI / I^2C subsystems – needed for management / monitoring functions at this stage; I^2C power also extends to the transition card.

5.8.1 Power Module

FIGURE 5-19 shows a schematic diagram of the power module. This subassembly is integrated with the Netra CP2300 board.

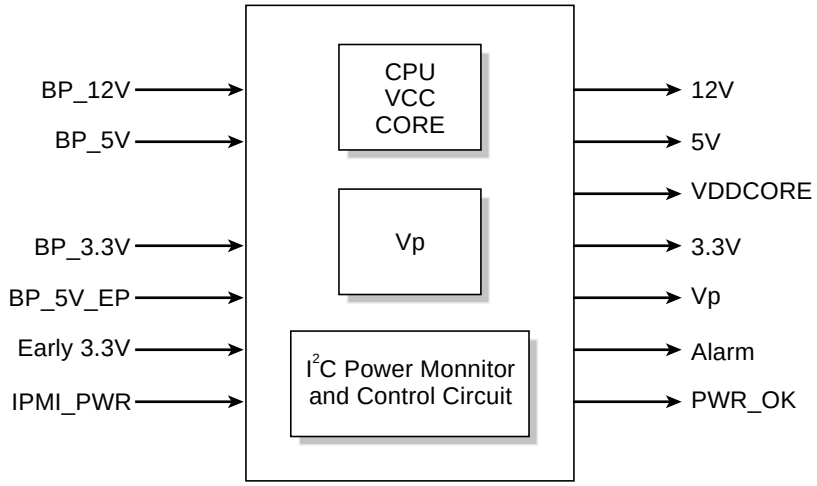

FIGURE 5-19 Power Module Interface

This subsystem performs the following functions:

- Generates Vp, the CompactPCI hot-swap precharge bias voltage using early power
- Generates VDDCORE, the UltraSPARC processor core voltage supply
- Controls and gates 5V, 12V, 3.3V and -12V
- Automatically shuts down in case of overcurrent or over / under voltage
- Asserts the PWR_MOD_OK signal

The power module is controlled by the SMC and the power on / off signal. Functions controlled include core voltage, and backend on or off state. There are also automatic controls within the power module, for example, overcurrent shutdown, and voltage regulation.

The power module has a DIP switch with preset default settings. These switches are for factory use only (see FIGURE 5-20 for location). You *must* not change DIP switch settings for positions 1 though 5. Switch position 6, however, can be used to set the firmware userflash and system flash settings. See Section B.5.1, “SW3 DIP Switch” on page B-20 for more information.

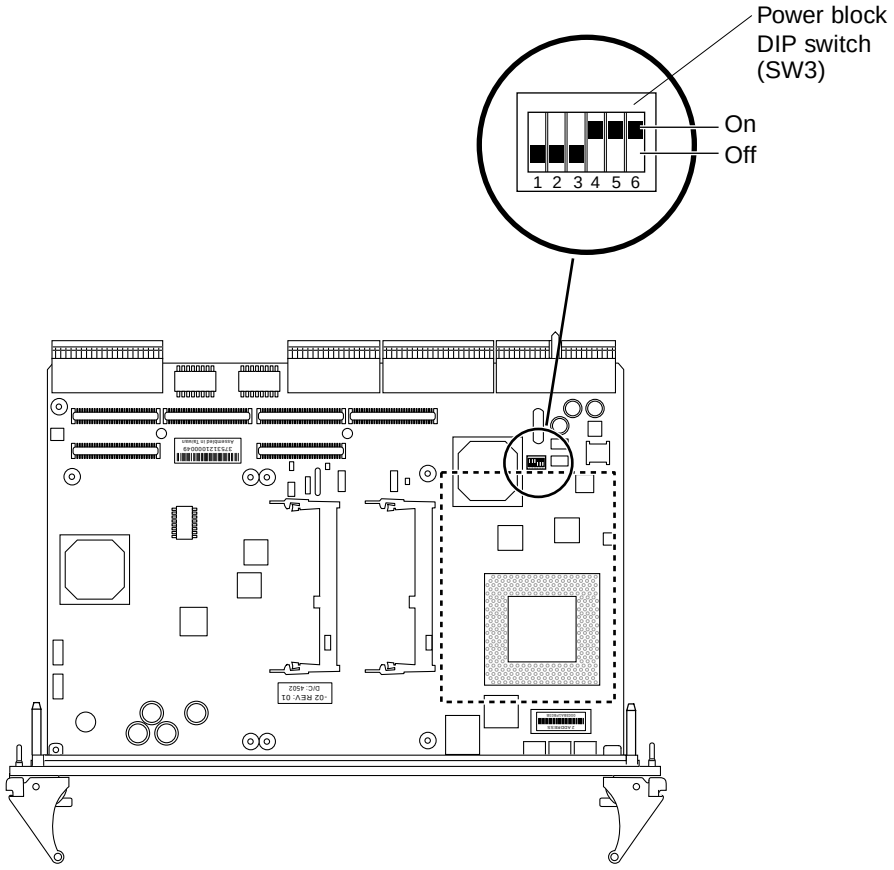

FIGURE 5-20 DIP Switch SW3 Settings on Power Block

5.8.2 Early Power and IPMI Power

If the system power for the backplane fails, the SMC can use IPMI power, typically supplied from an uninterruptible power supply (UPS), instead of early power from the cPSB backplane. The backplane is provided with IPMI power pins for this purpose. FIGURE 5-21 shows the circuit arrangement that selects between these power sources.

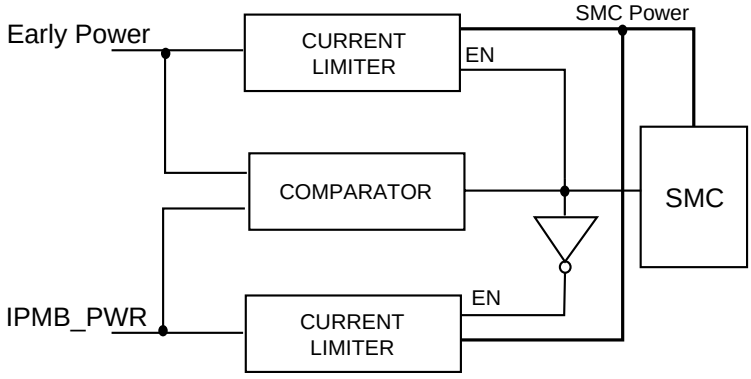

FIGURE 5-21 Selection Between Early Power and IPMI Power

5.8.3 Transition Card Power Distribution

FIGURE 5-22 shows the power rail routing to the transition card. The Netra CP2300 cPSB transition card is powered from the Netra CP2300 board rather than directly from the backplane. The transition card must always be connected to the backplane before the chassis is powered. Always install the transition card before the Netra CP2300 in the chassis. For details on using a transition card, see Chapter 2.

Note – TABLE 5-2 lists how the Netra CP2300 board labels the CompactPCI backplane connectors.

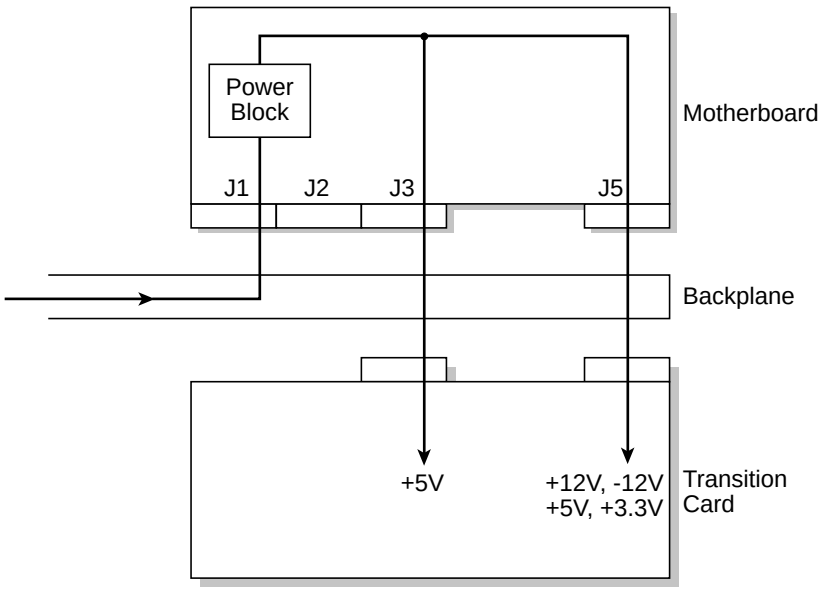

FIGURE 5-22 Transition Card Power Supply Routing

Note – Some V(I/O) power lines are routed into J2 of the motherboard; this is not shown in the figure for clarity.

5.9 CompactPCI Interface

This section provides information on CompactPCI and the Netra CP2300 board interface requirements specifications and CompactPCI signal interface.

5.9.1 CompactPCI Interface Requirements

TABLE 5-4 lists the requirements for Netra CP2300 boards as defined by the PICMG 3.0 CompactPCI and Netra CP2300 board design requirements specifications:

TABLE 5-4 Compact PCI Interface Requirements

Requirement	Description
Hot swap	Provide 1V +/-20% precharge bias voltage (Vp) for all required CompactPCI bus signals.

5.9.2 CompactPCI Signal Interface

This section lists the CompactPCI connector power signal interfaces.

TABLE 5-5 cPCI Connector Power Signal Interface

Voltage	cPCI Pin(s) (See TABLE 5-2 for Connector Labeling)	Net Name	Notes
3.3V	J1-C6 & C22	BP_EP_3.3V	Long pin
3.3V	J1-A15, A17, A19, A21, A23, C10, C18, & D25	EP_3.3V	Medium pin
5V	J1-D3 & D23	BP_EP_5V	Long pin
5V	J1-A1, A25, B2, B24, E1, & E25	EP_5V	Medium pin
+12V	J1-D1	BP_12V_POS	Medium pin
-12V	J1-B1	BP_12V_NEG	Medium pin
3.3V or 5V	J1-C4	BP_EP_VIO	Long pin
3.3V or 5V	J1-C8, J1-C16, J1-C24, J2-A4, J2-C5, J2-C7, J2-C9, J2-C11, J2-C13	EP_VIO	Medium pin

Note – The early power voltages supply critical circuits such as SMC, cPCI interface circuits, and power module control circuit.

5.10 Interrupts

The Netra CP2300 board interrupts are listed in TABLE 5-6. These are processed and encoded by the I-Chip2 ASIC. This device assigns equal priority to all interrupting devices. When two devices need servicing at the same time, the I-Chip prioritizes using its internal round-robin scheduling scheme. The resultant vector is passed to the processor as a 6-bit parallel word. The ultimate interrupt priority is resolved in the UltraSPARC IIi processor.

TABLE 5-6 Netra CP2300 Board Interrupt Mapping

I-Chip2 Input	Interrupt	Type	Priority	Offset
PCI5_INT3	Primary IDE Interface	Level-low	3	0x1A
PCI6_INT3	System Management	Level-low	3	0x1E
PCI7_INT1	NET0 Ethernet Interface	Level-low	5	0x06
PCI7_INT2	NET1 Ethernet Interface	Level-low	6	0x1C
PCI7_INT3	USB Port 1 Interface	Level-low	7	0x24
PCI4_INT0	PMC 0 INT A	Level-low	2	0x0A
PCI4_INT2	PMC 0 INT B	Level-low	1	0x0B
PCI6_INT0	PMC 0 INT C	Level-low	6	0x0C
PCI3_INT0	PMC 0 INT D	Level-low	4	0x15
PCI2_INT3	PMC 1 INT A	Level-low	3	0x16
OBIO0_INT0	PMC 1 INT B	Level-low	3	0x20
OBIO0_INT2	PMC 1 INT C	Level-low	2	0x22
OBIO0_INT9	PMC 1 INT D	Level-low	8	0x27
PCI1_INT2	TTYA / B	Level-low	6	0x10
PCI3_INT3	SPARC_INT_L	Level-low	7	0x04

5.11 Chip-Select PLD Registers

TABLE 5-7 lists the chip-select programmable logic device (PLD) registers.

TABLE 5-7 Chip-Select PLD Registers

Address	R/W	Name	Bit	Description	Default
0xFF00	R/O	N/A	7:4	Unused	0000
	R/W	IP_PW	3	This bit is not used in the current PLD	1
	R/W	RESUME_RST	2	This bit is not used in the current PLD	0
	R/W	FP_GREEN_LED	1:0	• 00: LED pulses heartbeat • 01: LED On solid • 10: LED flashes square wave @ 2Hz, 50 percent duty cycle • 11: LED is OFF	01
0xFF01	R/O	N/A	7:5	Unused	000
	R/W	PMC_BUSMODE[4:2]	4:2	• Bit 4 = PMC_BUSMODE4 • Bit 3 = PMC_BUSMODE3 • Bit 2 = PMC_BUSMODE2	000
	R/O	PMC_BUSMODEB, PMC_BUSMODEA	1:0	• Bit 1 = PMC_BUSMODEB • Bit 0 = PMC_BUSMODEA	11
0xFF03	R/O	PLD_REV	7:0	This register returns the revision of the PLD code during read	0001 0001
0xFF04	R/O	USER FLASH ADDRESS	7:4	It stores the upper 4 user flash address bits: • Bit 7: XD_INTEL_AD23 • Bit 6: XD_INTEL_AD22 • Bit 5: XD_INTEL_AD21 • Bit 4: XD_SA20	N/S
	R/O	GPO_FSH_ID	3	This bit is not used in the current PLD. It latches in the status of GPO_FSH_ID during reset	N/S
	R/W	Config Block Selection	2	Config Block Bit • `1` = boot from user flash, address is determined by bit 7 to 4 of this register • `0` = boot from boot flash	0

TABLE 5-7 Chip-Select PLD Registers *(Continued)*

Address	R/W	Name	Bit	Description	Default
	R/O	LPC_XBUS_CSR	1	Boot Block Selection, this bit returns the current state of LPC_XBUS_CSR • 1 = Use bit 2 (Config Block Bit) of this register to determine which user flash block to boot from: • 0 = boot from boot flash	N/S
	R/O	CTRL_JMP	0	Flash ROM Chip Select, this bit returns the current state of CTRL_JMP: • 1 = boot from on-board flash, will assert XD_FLASH_CE0_L when LPC_XBUS_CS is active; • 0 = boot from ROMBO, will assert PLD_FLASH_CS when LPC_XBUS_CS is active.	N/S
0xFF07	R/O	PWRGD	7	This bit returns the current status of PWRGD during read • 1 = VRM power is OK • 0 = VRM power is OFF	N/S
	R/O	MIC2580_PWRGD	6	This bit returns the current status of the inverted MIC2580_PWRGD during read • 1 = MIC2580 power is not OK • 0 = MIC2580 power is OK	N/S
	R/O	FP_POR_L	5	This bit returns the current status of the front panel power on reset pushbutton during read • 1 = FP_POR_L is de-asserted • 0 = FP_POR_L is asserted	N/S
	R/O	PLD_PB_XIR_L	4	This bit returns the current status of the PLD externally initiated reset pushbutton during read • 1 = PLD_PB_XIR_L is de-asserted • 0 = PLD_PB_XIR_L is asserted	N/S
	R/O	PCI_RESET_L	3	This bit returns the current status of the PCI_RESET_L during read • 1 = PCI_RESET_L is de-asserted • 0 = PCI_RESET_L is asserted	N/S
	R/O	SBRG_IDE_RST_L	2	This bit returns the current status of the SBRG_IDE_RST_L during read • 1 = SBRG_IDE_RST_L is de-asserted • 0 = SBRG_IDE_RST_L is asserted	N/S

TABLE 5-7 Chip-Select PLD Registers *(Continued)*

Address	R/W	Name	Bit	Description	Default
	R/O	SBRG_RST_L	1	This bit returns the current status of the SBRG_RST_L during read • 1 = SBRG_RST_L is de-asserted • 0 = SBRG_RST_L is asserted	N/S
	R/O	CPCI_RST_L	0	This bit returns the current status of the CPCI_RST_L during read\ • 1 = CPCI_RST_L is de-asserted • 0 = CPCI_RST_L is asserted	N/S
0XFF09	R/W	CPU_XIR_RST_SET	7	• 1 = Assert CPU_XIR_RST_L • 0 = De-assert CPU_XIR_RST_L	1
	R/W	CPU_POR_RST_SET	6	• 1 = Assert CPU_POR_RST_L • 0 = De-assert CPU_POR_RST_L	1
	R/W	CPU_SYS_RST_SET	5	• 1 = Assert CPU_SYS_RST_L • 0 = De-assert CPU_SYS_RST_L	1
	R/W	IDE_RST_SET	4	• 1 = Assert IDE_RST_L • 0 = De-assert IDE_RST_L	1
	R/W	SMC_RST_MAIN_SET	3	• 1 = Assert SMC_RST_MAIN_L • 0 = De-assert SMC_RST_MAIN_L	0
	R/W	I2C_RST_SET	2	• 1 = Assert I2C_RST_L • 0 = De-assert I2C_RST_L	1
	R/W	MIC2580_PW_ON_OFF	1	• 1 = Assert MIC2580_PW_ON_OFF • 0 = De-assert MIC2580_PW_ON_OFF	0
	R/W	VDDCORE_PW_ON_OFF	0	• 1 = Assert VDDCORE_PW_ON_OFF • 0 = De-assert VDDCORE_PW_ON_OFF	0

APPENDIX **A**

Specifications

Specifications for the Netra CP2300 board are provided in the following sections:

A.1 System Compatibility Specifications

Property	Specification
H110 chassis compatible	CompactPCI J4 is unconnected at the board; which enables this board to be used in H110 chassis
NEBS compliance	NEBS Level 3 specification compliance
CompactPCI compliance	• PICMG 2.16 CompactPCI Packet Switched Backplane specification • PICMG 2.1 R1.0 Hot Swap specification • PICMG 2.9 System Management specification

A.1.1 CompactPCI Specification Notes

PICMG 2.0 Rev 3 and IEEE 1101.10-1996 requires 2.54mm between the top of components and the separation plane, and there is at least approximately 0.5mm to 2mm of clearance to solder-side components or leads of an adjacent board from that same separation plane. Therefore, there is very little chance that a small specification violation will impact an adjacent card in a PICMG 2.0 Rev 3 compliant chassis.

Care should be taken when installing the boards in systems that have extreme solder-side component heights or in system chassis that do not allow clearances specified in the PICMG or IEEE standards.

The Netra CP2300 board also has a solder side cover installed. The components on the solder side cover meet the limits of the cPCI specification for maximum height. The solder side cover is nominally 1mm thick. When this cover rests upon components greater than 1mm in height, the cover itself may violate the cPCI specification where it rests on these components.

A.2 CPU Specifications

TABLE A-1 CPU Specification

Property	Specification
CPU	650 MHz UltraSPARC IIi
Mounting	370-pin ceramic PGA package soldered to board
Architecture	Sun 4U; 64-bit SPARC V9 architecture with the VIS instruction set
Cache	Integrated, 512 Kbyte, 4-way, set-associative internal L2 cache operating in 2:2 mode
PCI bus local interface	PCI Bus 2.1 compatible, 33/66 MHz, 32-bit, 3.3V (internal to board only)

A.3 Main Memory Specifications

TABLE A-2 Memory Specification

Property	Specification
Memory size—min	512 MB on-board memory
Memory size—max.	1.5 GB (512 MB on-board memory plus two 512 MB SO-DIMM memory modules)
Onboard memory	512 MB on-board memory
Memory type	3.3V, synchronous DRAM with ECC LVTTL-compatible CMOS; configured on bus width of 64-bit + 8-ECC bits
Identification to system	Serial EEPROM provides serial presence detect (SPD)
CAS latency	CAS Latency 2 (CL2)
SDRAM characteristics	PC133-Compliant, unregistered and unbuffered
ECC	8-bit; single bit error correction; double-bit error detection

A.4 Memory Configuration Specifications

The Netra CP2300 board contains 512 MBytes of on-board SDRAM memory. The board also contains two connectors for PC133 ECC SO-DIMM memory expansion (see Section 2.4.1, “Installing SO-DIMM Memory Modules” on page 2-6 for installation instructions).

The Netra CP2300 board supports SO-DIMM memory modules that match the following characteristics:

- 144-pin ECC SO-DIMMs that conform to the JEDEC 21-C standard
- Memory data bus width: 64 bit data, 8 bit ECC
- PC133-compliant SDRAM
- CAS Latency 2 (CL2)
- Serial presence detect (SPD) support required
- Unregistered and Unbuffered

The low profile memory connectors of the CP2300-650-512MBLP configuration will accept SO-DIMM memory modules, with heights 31.75 mm (1.25 in.) or less, that meet the JEDEC 21-C standard. The larger memory connectors of the CP2300-650-512MB configuration will accept SO-DIMM memory modules that exceed the standard’s width dimension by 1.2 mm (.04 in.).

FIGURE A-1 and TABLE A-3 show the allowable mechanical dimensions of SO-DIMM memory modules for each board configuration.

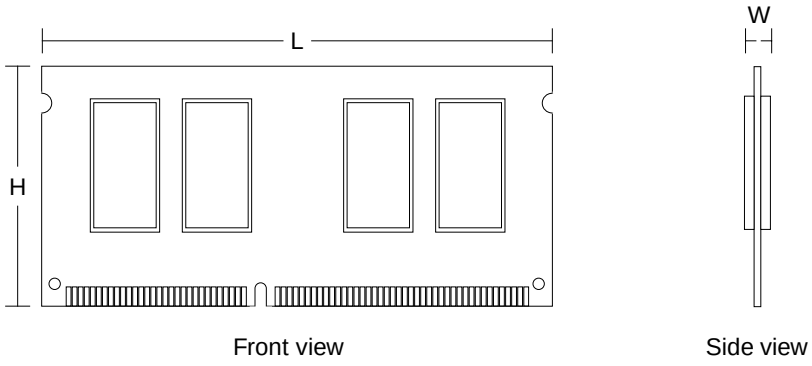

FIGURE A-1 SO-DIMM Memory Module Dimensions

TABLE A-3 Allowable SO-DIMM Physical Dimensions

Board Configuration	Connector Type	Physical Dimensions of Allowable SO-DIMM Modules
CP2300-650-512MBLP	Low profile	31.75 mm (1.25 in.) H x 67.60 mm (2.66 in.) L x 4.00 mm (.15 in.) W
CP2300-650-512MB	Regular	31.75 mm (1.25 in.) H x 67.60 mm (2.66 in.) L x 5.20 mm (.20 in.) W

TABLE A-4 lists the SO-DIMM memory size and configurations.

TABLE A-4 SO-DIMM Memory Configurations

SO-DIMM Memory Size	Configuration	SDRAM Device Size	Number of Chips on Each SO-DIMM	Memory Size of Two SO-DIMMs	Total Memory Capacity (Including 512 MB On-Board Memory)
64 MB	8M x 72	64 Mbit	9	128 MB	640 MB
128 MB	2 x 8M x 72	64 Mbit	18	256 MB	768 MB
128 MB	16M x 72	128 Mbit	9	256 MB	768 MB
256 MB	2 x 16M x 72	128 Mbit	18	512 MB	1024 MB (1 GB)
512 MB	2 x 32M x 72	256 Mbit	18	1 GB	1536 MB (1.5 GB)
1 GB	2 x 64M x 72	512 Mbit	18	2 GB	2560 MB (2.5 GB)

A.5 PMC Interface Specifications

TABLE A-5 PMC Interface Specification

Property	Specification
PMC module interfaces on system board	Two interfaces at PMC A and PMC B
Interface IEEE P1386.1 compliance	With draft 2.1
Connector configuration, PMC A (P1386 designations)	Jn1 (J5), Jn2 (J7) carry PCI signals; Jn4 (J7) module I/O is connected to the CompactPCI J3 (J13) backplane connector
Connector configuration, PMC B (P1386 designations)	Jn1 (J6), Jn2 (J12) carry PCI signals; Jn4 (J11) module I/O is connected to the CompactPCI J5 (J14) backplane connector

TABLE A-5 PMC Interface Specification *(Continued)*

Property	Specification
PCI clock	33 MHz
PCI bus width	32-bit
Max power load -- per module, combined power rails (5V, 3.3V, 12V, -12V)	7.5 W

A.5.1 PMC Specification Notes

The regular SO-DIMM memory connectors on the CP2300-650-512MB configuration may interfere with PMC cards installed in PMC slot A, as these tall connectors do not meet the PMC clearance specification (they are 0.5 mm out of clearance).

When at all possible, install PMC cards that exceed PMC component height restrictions in the PMC A slot. PMC disk drive cards in particular may impact the memory connectors on PMC A, as some commercially available PMC disk cards exceed component height and/or thermal restrictions.

The low profile SO-DIMM memory connectors on the CP2300-650-512MBLP board configuration meet the PMC clearance specification.

A.6 Power Requirements

This section provides information on power sequencing and power requirements by connection phase. TABLE A-6 shows the power drawn from the backplane connector by phase.

TABLE A-6 Netra CP2300 Backplane Connector Power Requirements by Connection Phase

Power Rail	No BP Power	Early power on long pins* Typical (A)	Main power on medium pins:† Typical (with 512MB on-board total memory)	Main power on medium pins: Typical (with two 512MB SO-DIMMs installed)‡	Description
+5V	0	0.35	3.0A average (3.5A peaks)	3.0A average (3.5A peaks)	At CompactPCI connectors J1(J9) / J2(J10)
+3.3V	0	0.02	1.5A average (2.2A peaks)	3.4A average (3.3A peaks)	At CompactPCI connectors J1(J9) / J2(J10)
+12V	0	0.00	15mA	15mA	At CompactPCI connectors J1(J9) / J2(J10)
–12V	0	0.00	15mA	15mA	At CompactPCI connectors J1(J9) / J2(J10)
IPMB_PWR	0.15	0	0	0	At CompactPCI connector J1(J9) / A4

* The typical figures provided for early power are only provided as examples.

† The typical figures are calculated as measured on a similar board, no PMC cards, with or without the Netra CP2300 cPSB Transition Card and while running the SunVTS system exerciser.

‡ The maximum memory supported is up to 2.5 GB.

A.7 Mechanical Specifications

The Netra CP2300 board's front panel meets the mechanical specifications found in the CompactPCI specification PICMG 2.0 R3.0. See Appendix D for a reference to this specification. FIGURE A-2 shows a mechanical illustration of the Netra CP2300 board panel.

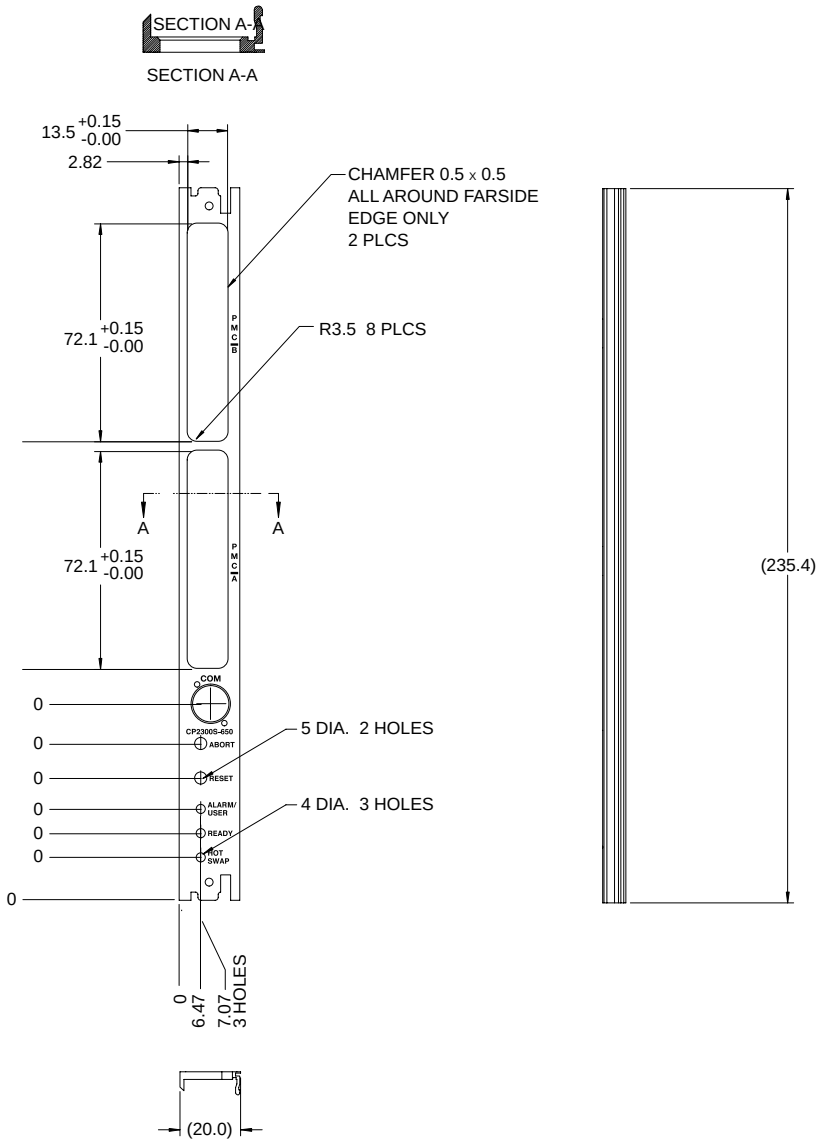

FIGURE A-2 Mechanical Illustration of the Netra CP2300 Front Panel

A.8 Environmental Specifications

TABLE A-7 Environmental Conditions and Limits

Ambient Conditions	Low Limit*	High Limit
Transportation and Storage Temperature	-40^0 C	+70^0 C
Transportation and Storage Humidity	5% RH† non-condensing	95% RH non-condensing
Operating Temperature	0^0 C (-5^0 C short term)	40^0 C (55^0 C short term)
Operating Humidity	15% RH non-condensing	85% RH (90% RH short term) non-condensing
Shock and Vibration	As stated in NEBS GR-63 CORE specifications, section 4.3.1 and 4.3.2 for shock criteria and 4.4.3 for vibration criteria; MIL-STD 810E, Method 514.4, CAT I MIL-STD 810E, Method 516.4, II-3.2	
Electrostatic Discharge	NEBS GR-1089 Section 2	

* Short term, in this column, refers to a period of not more than 96 consecutive hours and a total of not more than 15 days in 1 year.

† RH is relative humidity.

A.9 Thermal Validation

The CPU diode temperature should not exceed 85^0 C when installed in the system. Refer to the *Netra CP2300 cPSB Board Programming Guide* (816-1331-*xx*) for more information on thermal validation.

A.10 Reliability / Availability Specifications

Reliability, availability and serviceability (RAS) specifications for the Netra CP2300 cPSB board are available through the Sun Sales office under a non-disclosure agreement.

A.11 Compliance Specifications

A.11.1 Agency Compliance

All printed wiring boards (PWBs) are manufactured by UL recognized manufacturers, and have a flammability rating of 94-V0 or better.

Compliance with EMI and safety regulations for products including the Netra CP2300 board is entirely the responsibility of OEMs. The Netra CP2300 board has passed FCC Class A tests in representative enclosures. However, the EMI Class of the end use system is dependent upon system level EMI design parameters.

The Netra CP2300 boards are intended to be incorporated into systems meeting the following regulations and compliances:

- USA FCC part 15
- USA Safety UL 60950
- Canadian EMI ICES-003
- Canadian Safety CSA C22.2 Number 60950
- European Union EMC CE Mark EN55022, EN555024 and EN300-386 v1.3.1
- European Union Low Voltage Directive Safety CE Mark EN 60950
- Japanese EMI VCCI
- Taiwanese EMI BSMI
- Korean EMI MIC

A.11.2 NEBS Level 3

Board requirements for NEBS Level 3 criteria provide the highest assurance of product operability with minimal service interruptions over the life of the equipment. The requirements include the following categories and all associated sections and subcategories:

- GR-63-CORE, Issue 1, October 1995 - Network Equipment-Building System Requirements: Physical Protection
- GR-1089-CORE, Issue 2, Revision 1, February 1999 - Electromagnetic Compatibility and Electrical Safety - Generic Criteria for Network Telecommunications Equipment

APPENDIX **B**

Connectors, Pinouts and Switch Settings

This chapter contains the following subsections:

Note – For pin assignments of the rear transition card connectors, refer to the transition card manual.

B.1 PMC Connectors

FIGURE B-1 shows the locations of PMC port connectors, and the tables below show contact allocations.

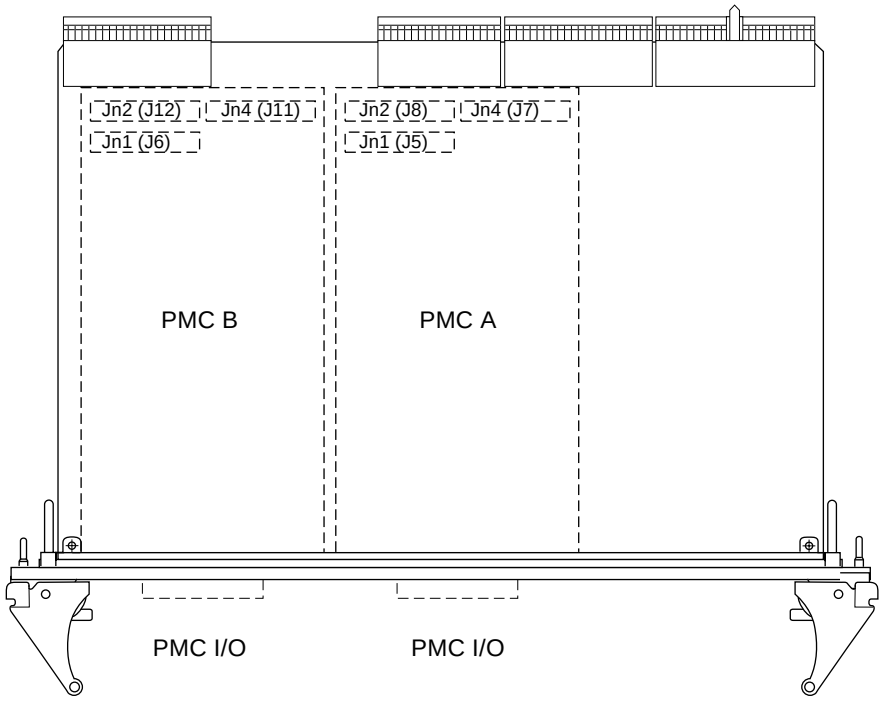

FIGURE B-1 Netra CP2300 Board PMC Port Connectors

Note – The P1386.1 standard reserves the Jn3 64-pin connector for PCI 64-bit extensions, so it is not fitted on the Netra CP2300 board.

TABLE B-1 lists how the PMC slot connectors are labelled on the board.

TABLE B-1 PMC Connector Labelling

PMC Slot	PMC Connector	Board Connector Label
PMC slot B	Jn1	J6
PMC slot B	Jn2	J12
PMC slot B	Jn4	J11
PMC slot A	Jn1	J5
PMC slot A	Jn2	J8
PMC slot A	Jn4	J7

B.1.1 PMC A Connector Interfaces

Corresponding to the Common Mezzanine Card (CMC) specification, the PMC A slot is comprised of three PMC connectors: Jn1 (labeled J5 on the board), Jn2 (J8), and Jn4 (J7). (The Jn3 connector is not fitted on the Netra CP2300 board.)

The following tables list the PMC A slot connector interfaces.

TABLE B-2 PMC A Jn1 (J5) Connector Interface

Pin	Description	Pin	Description
1	TCK; JTAG clock signal.	2	-12V
3	GND	4	PMC_A_INT_A_L
5	PMC_A_INT_B_L	6	PMC_A_INT_C_L
7	PMC_BUSMODE1_L*	8	VCC (5V)
9	PMC_A_INT_D_L	10	NC
11	GND	12	NC
13	PMC_CLK	14	GND
15	GND	16	PMC_GNT_L
17	PMC_REQ_L	18	VCC
19	LOCAL_VIO	20	PCI_B_AD<31>
21	PCI_B_AD<28>	22	PCI_B_AD<27>
23	PCI_B_AD<25>	24	GND

TABLE B-2 PMC A Jn1 (J5) Connector Interface *(Continued)*

Pin	Description	Pin	Description
25	GND	26	PCI_B_CBE3_L
27	PCI_B_AD<22>	28	PCI_B_AD<21>
29	PCI_B_AD<19>	30	VCC
31	LOCAL_VIO	32	PCI_B_AD<17>
33	PCI_B_FRAME_L	34	GND
35	GND	36	PCI_B_IRDY_L
37	PCI_B_DEVSEL_L	38	VCC
39	GND	40	PCI_B_LOCK_L
41	PMC_SDONE	42	PMC_SB0_L
43	PCI_B_PAR	44	GND
45	LOCAL_VIO	46	PCI_B_AD<15>
47	PCI_B_AD<12>	48	PCI_B_AD<11>
49	PCI_B_AD<9>	50	VCC
51	GND	52	PCI_B_CBE_L<0>
53	PCI_B_AD<6>	54	PCI_B_AD<5>
55	PCI_B_AD<4>	56	GND
57	LOCAL_VIO	58	PCI_B_AD<3>
59	PCI_B_AD<2>	60	PCI_B_AD<1>
61	PCI_B_AD<0>	62	VCC
63	GND	64	PCI_B_REQ64_L

* BUSMODE signals require a pull-up

TABLE B-3 PMC A Jn2 (J8) Connector Interface

Pin	Description	Pin	Description
1	+12V	2	JTAG_PMC_RST_L
3	TMS	4	PMC_TDO
5	PMC_TDI	6	GND
7	GND	8	NC
9	NC	10	NC

TABLE B-3 PMC A Jn2 (J8) Connector Interface *(Continued)*

Pin	Description	Pin	Description
11	PMC_BUSMODE2_L	12	VDD (3.3V)
13	PCI_B_RST_L	14	PMC_BUSMODE3_L
15	VDD	16	PMC_BUSMODE4_L
17	NC	18	GND
19	PCI_B_AD<30>	20	PCI_B_AD<29>
21	GND	22	PCI_B_AD<26>
23	PCI_B_AD<24>	24	VDD
25	PCI_B_IDSEL	26	PCI_B_AD<23>
27	VDD	28	PCI_B_AD<20>
29	PCI_B_AD<18>	30	GND
31	PCI_B_AD<16>	32	PCI_B_CBE_L<2>
33	GND	34	NC
35	PCI_B_TRDY_L	36	VDD
37	GND	38	PCI_B_STOP_L
39	PCI_B_PERR_L	40	GND
41	VDD	42	PCI_B_SERR_L
43	PCI_B_CBE_L<1>	44	GND
45	PCI_B_AD<14>	46	PCI_B_AD<13>
47	GND	48	PCI_B_AD<10>
49	PCI_B_AD<8>	50	VDD
51	PCI_B_AD<7>	52	NC
53	VDD	54	NC
55	NC	56	GND
57	NC	58	NC
59	GND	60	NC
61	PCI_B_ACK64_L	62	VDD
63	GND	64	NC

Note – The P1386.1 standard reserves the Jn3 64-pin connector for PCI 64-bit extensions. It is not fitted on these boards.

TABLE B-4 PMC A Jn4 (J7) Connector Interface

Pin	Description
1-64	PMC_A_IO<1-64> are user defined IO pins

B.1.2 PMC B Connector Interfaces

Corresponding to the Common Mezzanine Card (CMC) specification, the PMC B slot is comprised of three PMC connectors: Jn1 (labeled J6 on the board), Jn2 (J12), and Jn4 (11). (The Jn3 connector is not fitted on the Netra CP2300 board.)

The following tables list the PMC B slot connector interfaces.

TABLE B-5 PMC B Jn1 (J6) Connector Interface

Pin	Description	Pin	Description
1	TCK; JTAG clock signal.	2	-12V
3	GND	4	PMC_B_INT_A_L
5	PMC_B_INT_B_L	6	PMC_B_INT_C_L
7	PMC_BUSMODE1_L	8	VCC (5V)
9	PMC_B_INT_D_L	10	NC
11	GND	12	NC
13	PMC_CLK	14	GND
15	GND	16	PMC_GNT_L
17	PMC_REQ_L	18	VCC
19	LOCAL_VIO	20	PCI_B_AD<31>
21	PCI_B_AD<28>	22	PCI_B_AD<27>
23	PCI_B_AD<25>	24	GND
25	GND	26	PCI_B_CBE3_L
27	PCI_B_AD<22>	28	PCI_B_AD<21>
29	PCI_B_AD<19>	30	VCC
31	LOCAL_VIO	32	PCI_B_AD<17>
33	PCI_B_FRAME_L	34	GND
35	GND	36	PCI_B_IRDY_L

TABLE B-5 PMC B Jn1 (J6) Connector Interface *(Continued)*

Pin	Description	Pin	Description
37	PCI_B_DEVSEL_L	38	VCC
39	GND	40	PCI_B_LOCK_L
41	PMC_SDONE	42	PMC_SB0_L
43	PCI_B_PAR	44	GND
45	LOCAL_VIO	46	PCI_B_AD<15>
47	PCI_B_AD<12>	48	PCI_B_AD<11>
49	PCI_B_AD<9>	50	VCC
51	GND	52	PCI_B_CBE_L<0>
53	PCI_B_AD<6>	54	PCI_B_AD<5>
55	PCI_B_AD<4>	56	GND
57	LOCAL_VIO	58	PCI_B_AD<3>
59	PCI_B_AD<2>	60	PCI_B_AD<1>
61	PCI_B_AD<0>	62	VCC
63	GND	64	PCI_B_REQ64_L

TABLE B-6 PMC B Jn2 (J12) Connector Interface

Description	Pin	Pin	Description
+12V	1	2	JTAG_PMC_RST_L
TMS	3	4	PMC_TDO
PMC_TDI	5	6	GND
GND	7	8	NC
NC	9	10	NC
PMC_BUSMODE2_L	11	12	VDD (3.3V)
PCI_B_RST_L	13	14	PMC_BUSMODE3_L
VDD	15	16	PMC_BUSMODE4_L
NC	17	18	GND
PCI_B_AD<30>	19	20	PCI_B_AD<29>
GND	21	22	PCI_B_AD<26>
PCI_B_AD<24>	23	24	VDD

TABLE B-6 PMC B Jn2 (J12) Connector Interface *(Continued)*

Description	Pin	Pin	Description
PCI_B_IDSEL	25	26	PCI_B_AD<23>
VDD	27	28	PCI_B_AD<20>
PCI_B_AD<18>	29	30	GND
PCI_B_AD<16>	31	32	PCI_B_CBE_L<2>
GND	33	34	NC
PCI_B_TRDY_L	35	36	VDD
GND	37	38	PCI_B_STOP_L
PCI_B_PERR_L	39	40	GND
VDD	41	42	PCI_B_SERR_L
PCI_B_CBE_L<1>	43	44	GND
PCI_B_AD<14>	45	46	PCI_B_AD<13>
GND	47	48	PCI_B_AD<10>
PCI_B_AD<8>	49	50	VDD
PCI_B_AD<7>	51	52	NC
VDD	53	54	NC
NC	55	56	GND
NC	57	58	NC
GND	59	60	NC
PCI_B_ACK64_L	61	62	VDD
GND	63	64	NC

Note – The P1386.1 standard reserves the Jn3 64-pin connector for PCI 64-bit extensions. It is not fitted on these boards.

TABLE B-7 PMC B Jn4 (J11) Connector Interface

Pin	Description
1-64	PMC_B_IO<1-64> are user defined IO pins

B.2 Memory Connector

Memory SO-DIMM pinouts match those called out in the JEDEC Standard No. 21-C,.4.5.6-2 ECC Mode SO-DIMM.

Note – The Netra CP2300 board does not support SO-DIMM slot pin 72 A13 = 0.

TABLE B-8 144-Pin SO-DIMM Memory Connector Pin Assignments

Pin	X64 DIMM Assignment	X72 ECC Mode DIMM Assignment	Pin	X64 DIMM Assignment	X72 ECC Mode DIMM Assignment	Pin	X64 DIMM Assignment	X72 ECC Mode DIMM Assignment
1	VSS		49	DQ13		97	DQ22	
2	VSS		50	DQ45		98	DQ54	
3	DQ0		51	DQ14		99	DQ23	
4	DQ32		52	DQ46		100	DQ55	
5	DQ1		53	DQ15		101	VDD	
6	DQ33		54	DQ47		102	VDD	
7	DQ2		55	VSS		103	A6	
8	DQ34		56	VSS		104	A7	
9	DQ3		57	NC	CB0	105	A8	
10	DQ35		58	NC	CB4	106	BA0	
11	VDD		59	NC	CB1	107	VSS	
12	VDD		60	NC	CB5	108	VSS	
13	DQ4		61	CK0		109	A9	
14	DQ36		61	CK0		110	BA1	
15	DQ5		62	CKE0		111	A10/AP	
16	DQ37		62	CKE0		112	A11	
17	DQ6		63	VDD		113	VDD	
18	DQ38		63	VDD		114	VDD	
19	DQ7		64	VDD		115	DQMB2	
20	DQ39		65	RAS		116	DQMB6	
21	VSS		66	CAS		117	DQMB3	

TABLE B-8 144-Pin SO-DIMM Memory Connector Pin Assignments *(Continued)*

Pin	X64 DIMM Assignment	X72 ECC Mode DIMM Assignment	Pin	X64 DIMM Assignment	X72 ECC Mode DIMM Assignment	Pin	X64 DIMM Assignment	X72 ECC Mode DIMM Assignment
22	VSS		67	W		118	DQMB7	
23	DQMB0		68	CKE1		119	VSS	
24	DQMB4		69	S0		120	VSS	
25	DQMB1		70	A12		121	DQ24	
26	DQMB5		71	S1		122	DQ56	
27	VDD		72	A13*, DSF		123	DQ25	
28	VDD		73	NU		124	DQ57	
29	A0		74	CK1		125	DQ26	
30	A3		75	VSS		126	DQ58	
31	A1		76	VSS		127	DQ27	
32	A4		77	NC, MWAIT	CB2, MWAIT	128	DQ59	
33	A2		78	NC, MIRQ	CB6, MIRQ	129	VDD	
34	A5		79	NC	CB3	130	VDD	
35	VSS		80	NC	CB7	131	DQ28	
36	VSS		81	VDD		132	DQ60	
37	DQ8		82	VDD		133	DQ29	
38	DQ40		83	DQ16		134	DQ61	
39	DQ9		84	DQ48		135	DQ30	
40	DQ41		85	DQ17		136	DQ62	
41	DQ10		86	DQ49		137	DQ31	
42	DQ42		87	DQ18		138	DQ63	
43	DQ11		88	DQ50		139	VSS	
44	DQ43		89	DQ19		140	VSS	
45	VDD		90	DQ51		141	SDA	
46	VDD		91	VSS		142	SCL	
47	DQ12		92	VSS		143	VDD	
48	DQ44		93	DQ20		144	VDD	

* The Netra CP2300 board does not support SO-DIMM slot pin 72 A13 = 0.

B.3 Front Panel Serial Connector

This section contains the connector pin assignments for the front panel serial port.

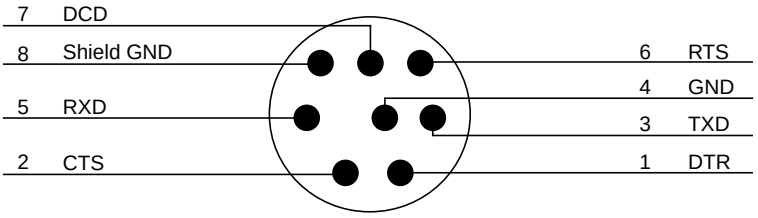

FIGURE B-2 Front Panel Serial Port (TTYA) Diagram

TABLE B-9 shows the serial port connector pin assignments.

TABLE B-9 Serial Mini Din 8-pin Connector Pinouts

Pin	Signal Name	Pin	Signal Name
1	FP_SER_A_DTR	5	FP_SER_A_RXD
2	FP_SER_A_CTS	6	FP_SER_A_RTS
3	FP_SER_A_TXD	7	FP_SER_A_DCD
4	FP_SER_A_GND	8	Shield GND

B.4 Backplane Connectors

FIGURE B-3 shows contact numbering as seen from the back of the Netra CP2300 board.

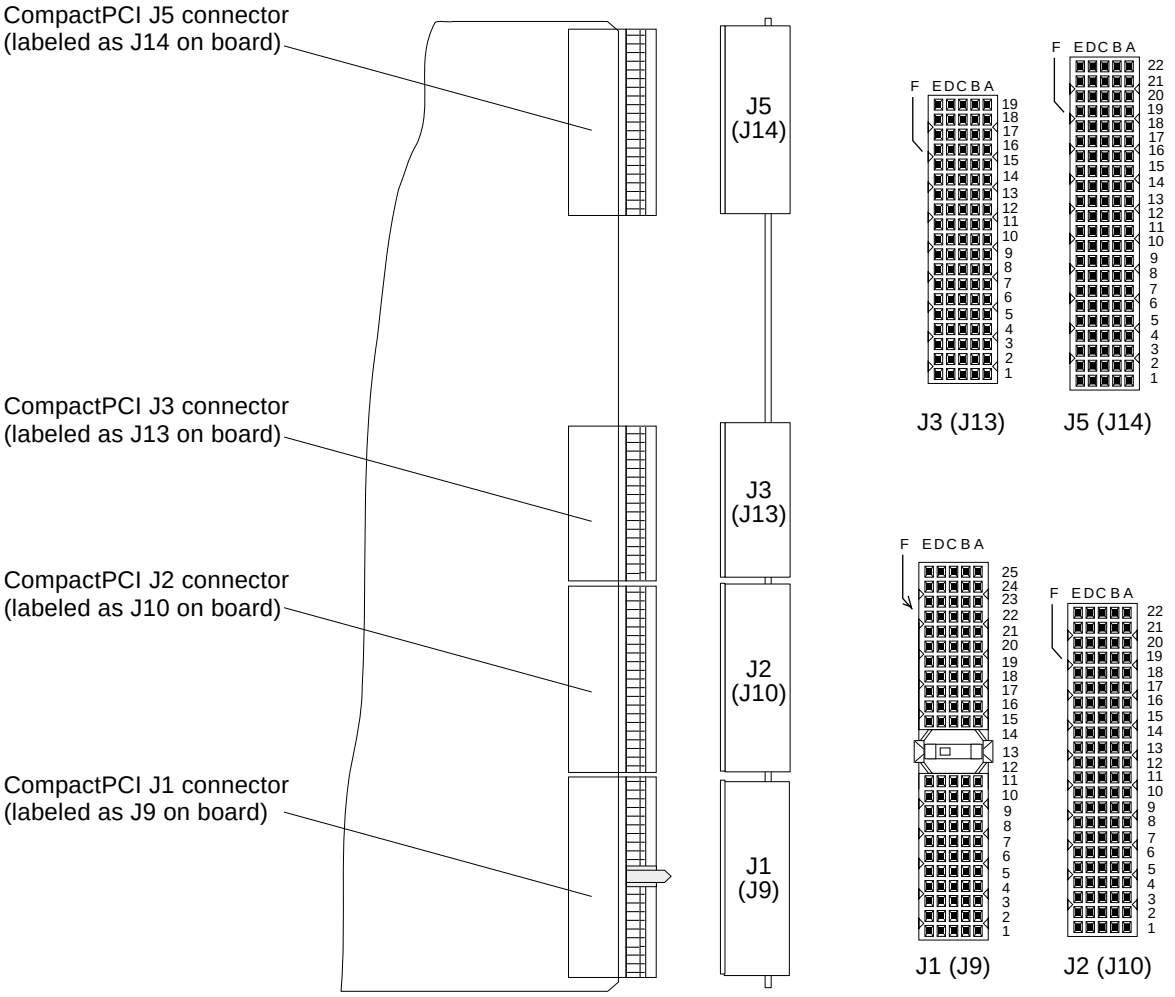

FIGURE B-3 Backplane Connector Contact Numbering

Note – The CompactPCI J4 connector is not populated on the Netra CP2300 board.

B.4.1 CompactPCI J1/P1 (J9) Connector Pinout

The CompactPCI J1 connector is labeled as J9 on the Netra CP2300 board.

TABLE B-10 CompactPCI J1/P1 (J9) Connector Pin Assignments

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
25	GND	+EP_5V	1Volt Prech.	VIO Prech.	+3.3V	+EP_5V	GND
24	GND	1Volt Prech.	+EP_5V	LP_VIO	1Volt Prech.	1Volt Prech.	GND
23	GND	EP_3.3V	1Volt Prech.	1Volt Prech.	LP_+EP_5V	1Volt Prech.	GND
22	GND	1Volt Prech.	GND	LP_+EP_3.3V	1Volt Prech.	1Volt Prech.	GND
21	GND	+EP_3.3V	1Volt Prech.	1Volt Prech.	1Volt Prech.	1Volt Prech.	GND
20	GND	1Volt Prech.	GND	VIO	1Volt Prech.	1Volt Prech.	GND
19	GND	+EP_3.3V	1Volt Prech.	1Volt Prech.	LP_GND	1Volt Prech.	GND
18	GND	1Volt Prech.	GND	+EP_3.3V	1Volt Prech.	1Volt Prech.	GND
17	GND	+EP_3.3V	**IPMB SCL**	**IPMB SDA**	LP_GND	1Volt Prech.	GND
16	GND	1Volt Prech.	GND	VIO	1Volt Prech.	1Volt Prech.	GND
15	GND	+EP_3.3V	1Volt Prech.	1Volt Prech.	**BD_SEL_L**	1Volt Prech.	GND
14	Key	Key	Key	Key	Key	Key	Key
13	Key	Key	Key	Key	Key	Key	Key
12	Key	Key	Key	Key	Key	Key	Key
11	GND	1Volt Prech.	1Volt Prech.	1Volt Prech.	LP_GND	1Volt Prech.	GND
10	GND	1Volt Prech.	GND	+EP_3.3V	1Volt Prech.	1Volt Prech.	GND
9	GND	1Volt Prech.	1Volt Prech.	1Volt Prech.	LP_GND	1Volt Prech.	GND
8	GND	1Volt Prech.	GND	VIO	1Volt Prech.	1Volt Prech.	GND
7	GND	1Volt Prech.	1Volt Prech.	1Volt Prech.	LP_GND	1Volt Prech.	GND
6	GND	1Volt Prech.	**PCI_PRES#**	LP_+EP_3.3V	1Volt Prech.	1Volt Prech.	GND
5	GND	BRSVP	BRSVP	PCI_RST#	LP_GND	1Volt Prech.	GND
4	GND	**IPMB_PWR**	**HEALTHY**	LP_VIO	**intp**	ints	GND
3	GND	VIO Prech.	VIO Prech.	VIO Prech.	LP_+EP_5V	VIO Prech.	GND
2	GND	**tck**	+EP_5V	tms	**tdo**	**tdi**	GND
1	GND	+EP_5V	-EP_12V	trst	+EP_12V	+EP_5V	GND

B.4.2 CompactPCI J1 / P1 (J9) Signal Descriptions

- 1 Volt Prech: Precharge to 1Volt through individual precharge pull-up resistors, these pins interface to the cPCI bus connector pins.
- VIO Prech: Precharge to EP_3.3V.
- +EP_5V: Backplane power input, EP_5V
- +EP_3.3V: Backplane power input, EP_3.3V
- +EP_12V: Backplane power input, EP_12V
- -EP_12V: Backplane power input, -EP_12V
- VIO: Backplane power input, can be either EP_3.3V or EP_5V
- LP_*: Long pins - see PCIMG Hot Swap Spec R2.0 section 4.2.1
- IPMB_SCL: Independent Platform Management Bus Clock - see CompactPCI System Management Specification PCIMG 2.9 R1.0
- IPMB_SDA: Independent Platform Management Bus Data - see CompactPCI System Management Specification PCIMG 2.9 R1.0
- BD_SEL#: PICMG 2.1 R1.0 Hot-swap signal - pulled up on the board and driven low to enable power on
- IPMB_PWR: Battery back-up power - see CompactPCI System Management Specification PCIMG 2.9 R1.0
- HEALTHY: Radial signal used to acknowledge the health of the board - signals that the board is suitable to be released form reset and allowed onto the bus - see PICMG 2.1 R1.0 Hotswap Spec.
- INTP: Non-cPCI interrupt, legacy IDE - not supported, 1Kohm pull-up provided
- INTS: Non-cPCI interrupt, legacy IDE - not supported
- TCK, TMS, TDO, TDI: JTAG signals, not supported - unconnected.
- BRSVP: Reserve pins - must be left unconnected on backplane
- PCI_PRES#: Used to indicate that the board is plugged into a chassis that supports the cPCI interface.
- PCI_RST#: cPCI interface reset input - in systems that do not support the cPCI interface a 10Kohm pulled is required on the backplane, needs to be pre-charged to VIO.

B.4.3 CompactPCI J2/P2 (J10) Connector Pinout

The CompactPCI J2 connector is labeled as J10 on the Netra CP2300 board.

TABLE B-11 CompactPCI J2/P2 (J10) Connector Pin Assignments

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	1Volt Prech.	GND	BRSVP	BRSVP	1Volt Prech.	GND
20	GND	1Volt Prech.	GND	1Volt Prech.	GND	1Volt Prech.	GND
19	GND	GND	GND	**SMB_SDA**	**SMB_SCK**	**SMB_ALERT**	GND
18	GND	BRSVP	BRSVP	1Volt Prech.	GND	BRSVP	GND
17	GND	BRSVP	GND	**PRST**#	1Volt Prech.	1Volt Prech.	GND
16	GND	BRSVP	BRSVP	**DEG#**	GND	BRSVP	GND
15	GND	BRSVP	GND	**FAL#**	1Volt Prech.	1Volt Prech.	GND
14	GND	1Volt Prech.	1Volt Prech.	1Volt Prech.	GND	1Volt Prech.	GND
13	GND	1Volt Prech.	GND	VIO	1Volt Prech.	1Volt Prech.	GND
12	GND	1Volt Prech.	1Volt Prech.	1Volt Prech.	GND	1Volt Prech.	GND
11	GND	1Volt Prech.	GND	VIO	1Volt Prech.	1Volt Prech.	GND
10	GND	1Volt Prech.	1Volt Prech.	1Volt Prech.	GND	1Volt Prech.	GND
9	GND	1Volt Prech.	GND	VIO	1Volt Prech.	1Volt Prech.	GND
8	GND	1Volt Prech.	1Volt Prech.	1Volt Prech.	GND	1Volt Prech.	GND
7	GND	1Volt Prech.	GND	VIO	1Volt Prech.	1Volt Prech.	GND
6	GND	1Volt Prech.	1Volt Prech.	1Volt Prech.	GND	1Volt Prech.	GND
5	GND	1Volt Prech.	1Volt Prech.	VIO	1Volt Prech.	1Volt Prech.	GND
4	GND	1Volt Prech.	BRSVP	1Volt Prech.	GND	1Volt Prech.	GND
3	GND	1Volt Prech.	GND	1Volt Prech.	1Volt Prech.	1Volt Prech.	GND
2	GND	1Volt Prech.	1Volt Prech.	**SYSEN#**	1Volt Prech.	1Volt Prech.	GND
1	GND	1Volt Prech.	GND	1Volt Prech.	1Volt Prech.	1Volt Prech.	GND

B.4.4 CompactPCI J2 / P2 (J10) Signal Descriptions

- GA[0..4]: Geographical Addressing signals for unique slot identification
- BRSVP: Reserve pins - leave unconnected on backplane
- SMB_SDA: System Management Data see PICMG 2.9 System Management Bus
- SMB_SCK: System Management Clock see PICMG 2.9 System Management Bus
- SMB_ALERT: cPCI System Management Specification PCIMG 2.9 R1.0 signal.
- PRST#: Backplane Push Button Reset input to the SMC
- DEG#, FAL#: Power Subsystem status signals input to the SMC
- SYSEN#: Used to indicate a slot's capability to support System Host

B.4.5 CompactPCI J3 / P3 (J13) Connector Pinout

The CompactPCI J3 connector is labeled as J13 on the Netra CP2300 board.

TABLE B-12 CompactPCI J3 / P3 (J13) Connector Pin Assignments

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
19	GND	RESERVE(GND)	RESERVE(GND)	RESERVE(GND)	RESERVE(GND)	GND	GND
18	GND	PSB_A_TX_POS	PSB_A_TX_NEG	GND	NC	NC	GND
17	GND	PSB_A_RX_POS	PSB_A_RX_NEG	GND	NC	NC	GND
16	GND	PSB_B_TX_POS	PSB_B_TX_NEG	GND	NC	NC	GND
15	GND	PSB_B_RX_POS	PSB_B_RX_NEG	GND	NC	NC	GND
14	GND	+3.3V	+3.3V	+3.3V	+5V	+5V	GND
13	GND	PMC_A_IO<5>	PMC_A_IO<4>	PMC_A_IO<3>	PMC_A_IO<2>	PMC_A_IO<1>	GND
12	GND	PMC_A_IO<10>	PMC_A_IO<9>	PMC_A_IO<8>	PMC_A_IO<7>	PMC_A_IO<6>	GND
11	GND	PMC_A_IO<15>	PMC_A_IO<14>	PMC_A_IO<13>	PMC_A_IO<12>	PMC_A_IO<11>	GND
10	GND	PMC_A_IO<20>	PMC_A_IO<19>	PMC_A_IO<18.	PMC_A_IO<17>	PMC_A_IO<16>	GND
9	GND	PMC_A_IO<25>	PMC_A_IO<24>	PMC_A_IO<23>	PMC_A_IO<22>	PMC_A_IO<21>	GND
8	GND	PMC_A_IO<30>	PMC_A_IO<29>	PMC_A_IO<28>	PMC_A_IO<27>	PMC_A_IO<26>	GND
7	GND	PMC_A_IO<35>	PMC_A_IO<34>	PMC_A_IO<33>	PMC_A_IO<32>	PMC_A_IO<31>	GND
6	GND	PMC_A_IO<40>	PMC_A_IO<39>	PMC_A_IO<38>	PMC_A_IO<37>	PMC_A_IO<36>	GND
5	GND	PMC_A_IO<45>	PMC_A_IO<44>	PMC_A_IO<43>	PMC_A_IO<42>	PMC_A_IO<41>	GND
4	GND	PMC_A_IO<50>	PMC_A_IO<49>	PMC_A_IO<48>	PMC_A_IO<47>	PMC_A_IO<46>	GND

TABLE B-12 CompactPCI J3/P3 (J13) Connector Pin Assignments

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
3	GND	PMC_A_IO<55>	PMC_A_IO<54>	PMC_A_IO<53>	PMC_A_IO<52>	PMC_A_IO<51>	GND
2	GND	PMC_A_IO<60>	PMC_A_IO<59>	PMC_A_IO<58>	PMC_A_IO<57>	PMC_A_IO<56>	GND
1	GND	+5V	PMC_A_IO<64>	PMC_A_IO<63>	PMC_A_IO<62>	PMC_A_IO<61>	GND

B.4.6 CompactPCI J3/P3 (J13) Signal Descriptions

- PMC_A[63..0] - PMC/PIM I/O signals
- TPE_A/B_TX/RX_POS/NEG: PCIMG CPSB Node Slot Ethernet Twisted Pair signals (PICMG 2.16 Draft 0.92 CompactPCI Packet Switching Backplane)
- +5V: Backend (SPARC) power VCC
- VDD_3.3V: Backend (SPARC) power 3.3V
- PMC_A_IO<29..1> may also be switched to EIDE port use mutually exclusive with using these pins as PMC_A_IO signals.

B.4.7 CompactPCI J5/P5 (J14) Connector Pinout

The CompactPCI J5 connector is labeled as J14 on the Netra CP2300 board.

TABLE B-13 CompactPCI J5/P5 (J14) Connector Pin Assignments

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
22	GND	PMC_B_IO<5>	PMC_B_IO<4>	PMC_B_IO<3>	PMC_B_IO<2>	PMC_B_IO<1>	GND
21	GND	PMC_B_IO<10>	PMC_B_IO<9>	PMC_B_IO<8>	PMC_B_IO<7>	PMC_B_IO<6>	GND
20	GND	PMC_B_IO<15>	PMC_B_IO<14>	PMC_B_IO<13>	PMC_B_IO<12>	PMC_B_IO<11>	GND
19	GND	PMC_B_IO<20>	PMC_B_IO<19>	PMC_B_IO<18>	PMC_B_IO<17>	PMC_B_IO<16>	GND
18	GND	PMC_B_IO<25>	PMC_B_IO<24>	PMC_B_IO<23>	PMC_B_IO<22>	PMC_B_IO<21>	GND
17	GND	PMC_B_IO<30>	PMC_B_IO<29>	PMC_B_IO<28>	PMC_B_IO<27>	PMC_B_IO<26>	GND
16	GND	PMC_B_IO<35>	PMC_B_IO<34>	PMC_B_IO<33>	PMC_B_IO<32>	PMC_B_IO<31>	GND
15	GND	PMC_B_IO<40>	PMC_B_IO<39>	PMC_B_IO<38>	PMC_B_IO<37>	PMC_B_IO<36>	GND
14	GND	PMC_B_IO<45>	PMC_B_IO<44>	PMC_B_IO<43>	PMC_B_IO<42>	PMC_B_IO<41>	GND
13	GND	PMC_B_IO<50>	PMC_B_IO<49>	PMC_B_IO<48>	PMC_B_IO<47>	PMC_B_IO<46>	GND
12	GND	PMC_B_IO<55>	PMC_B_IO<54>	PMC_B_IO<53>	PMC_B_IO<52>	PMC_B_IO<51>	GND
11	GND	PMC_B_IO<60>	PMC_B_IO<59>	PMC_B_IO<58>	PMC_B_IO<57>	PMC_B_IO<56>	GND
10	GND	RESERVE	PMC_B_IO<64>	PMC_B_IO<63>	PMC_B_IO<62>	PMC_B_IO<61>	GND
9	GND	SER_A_RTS	SER_A_DTR	SER_A_RI	GND	SER_A_CTS	GND
8	GND	SER_A_DCD	SER_A_TXD	SER_A_RXD	SER_A_DSR	+5V	GND
7	GND	SER_B_RTS	SER_B_DTR	SER_B_RI	SER_B_DSR	SER_B_CTS	GND
6	GND	SER_B_DCD	SER_B_TXD	SER_B_RXD	GND	GND	GND
5	GND	TXN_I2C_CLK	RESERVE	-12V	**(NET2_RX_P)**	**(NET2_RX_N)**	GND
4	GND	TXN_I2C_SDA	SMC_PWR	GND	**(NET2_TX_P)**	**(NET2_TX_N)**	GND
3	GND	**(USB_B_POS)**	(USB_B_NEG)	GND	GND	GND	GND
2	GND	USB_A_POS	USB_A_NEG	GND	**(NET1_RX_P)**	**(NET1_RX_N)**	GND
1	GND	GND	3.3V	+12V	**(NET1_TX_P)**	**(NET1_TX_N)**	GND

B.4.8 CompactPCI J5/P5 (J14) Signal Descriptions

- PMC_B[63..0] - PMC/PIM I/O signals
- +5V: Backend (SPARC) power VCC
- SMC_PWR: Early Power Plane to SMC, 5V for Transition Card I2C Devices
- TXN_I2C_SCL/SDA: I2C data and clock
- VDD_3.3V: Backend (SPARC) power 3.3V
- SER_A/B_RTS: Serial Port TTYA/B Request To Send
- SER_A/B_CTS: Serial Port TTYA/B Clear To Send
- SER_A/B_TX: Serial Port TTYA/B Transmit Data
- SER_A/B_RX: Serial Port TTYA/B Transmit Data
- SER_A/B_DCD: Serial Port TTYA/B Data Carrier Detected
- SER_A/B_DSR: Serial Port TTYA/B Data Set Ready
- SER_A/B_DTR: Serial Port TTYA/B Data Terminal Ready
- SER_A/B_RI: Serial Port TTYA/B Ring Indicator

B.5 DIP Switch Settings

The Netra CP2300 board contains two banks of DIP switches. The SW3 DIP switch is located on the component side of the board and the SW501, SW502, and SW503 DIP switches are located on the solder-side of the board.

B.5.1 SW3 DIP Switch

The SW3 DIP switch is a six position switch located on the component side of the Netra CP2300 board. FIGURE B-4 shows the location and default settings of the SW3 DIP switch.

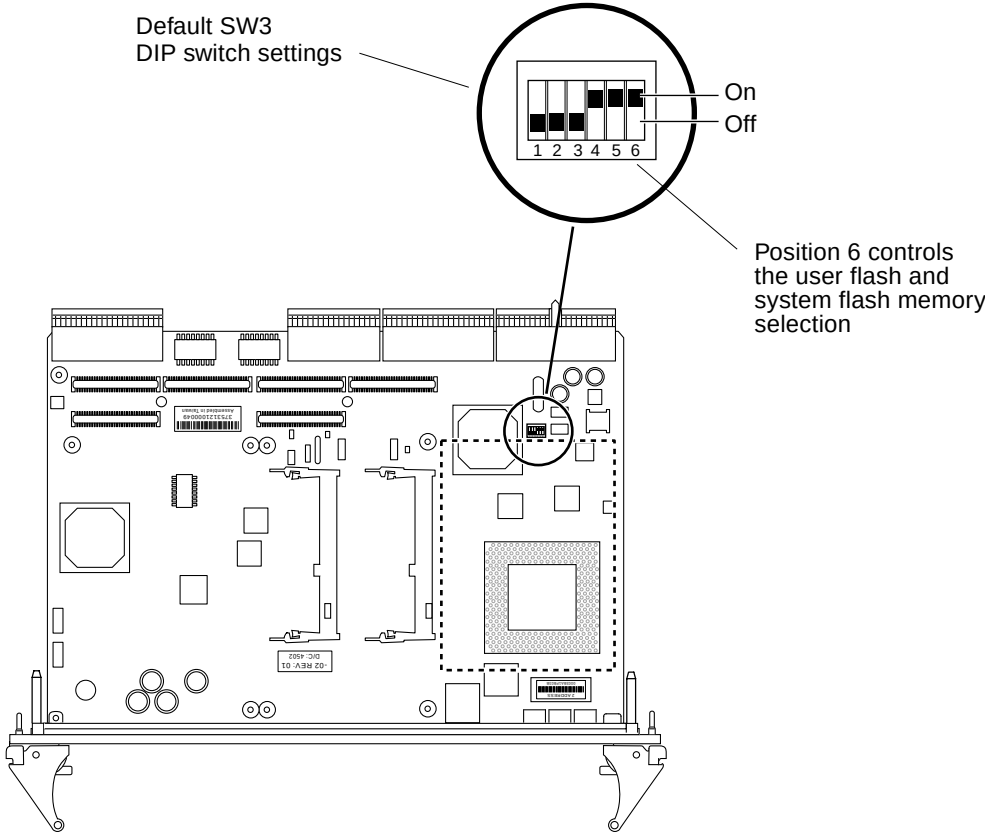

FIGURE B-4 SW3 DIP Switch Location and Default Settings

TABLE B-14 SW3 Position Settings

Position #	Default Setting	Description
1	OFF	Proprietary setting. Do not change setting.
2	OFF	Proprietary setting. Do not change setting.
3	OFF	Proprietary setting. Do not change setting.
4	ON	Proprietary setting. Do not change setting.
5	ON	Proprietary setting. Do not change setting.
6	ON	• ON = Boot the Netra CP2300 board from the standard OpenBoot PROM system flash. • OFF = Use the SMC firmware programmable variable `flash-device` to set whether the system flash is selected as bootable in 1 MByte or 7 MBytes of flash memory space.

For more information about switching the memory selection between the system flash and the user flash, see Section 4.7.1, “Exchanging the System and User Flash Memory Devices” on page 4-20.

Caution – SW3 DIP switch positions 1 through 5 are not user-selectable and must *never* be changed. Changing these settings may critically damage the Netra CP2300 board.

B.5.2 SW501, SW502, and SW503 DIP Switches

The SW501, SW502, and SW503 DIP switches are ten position switches located on the solder side of the Netra CP2300 board. FIGURE B-5 shows the location and default settings of the SW501, SW502, and SW503 DIP switches.

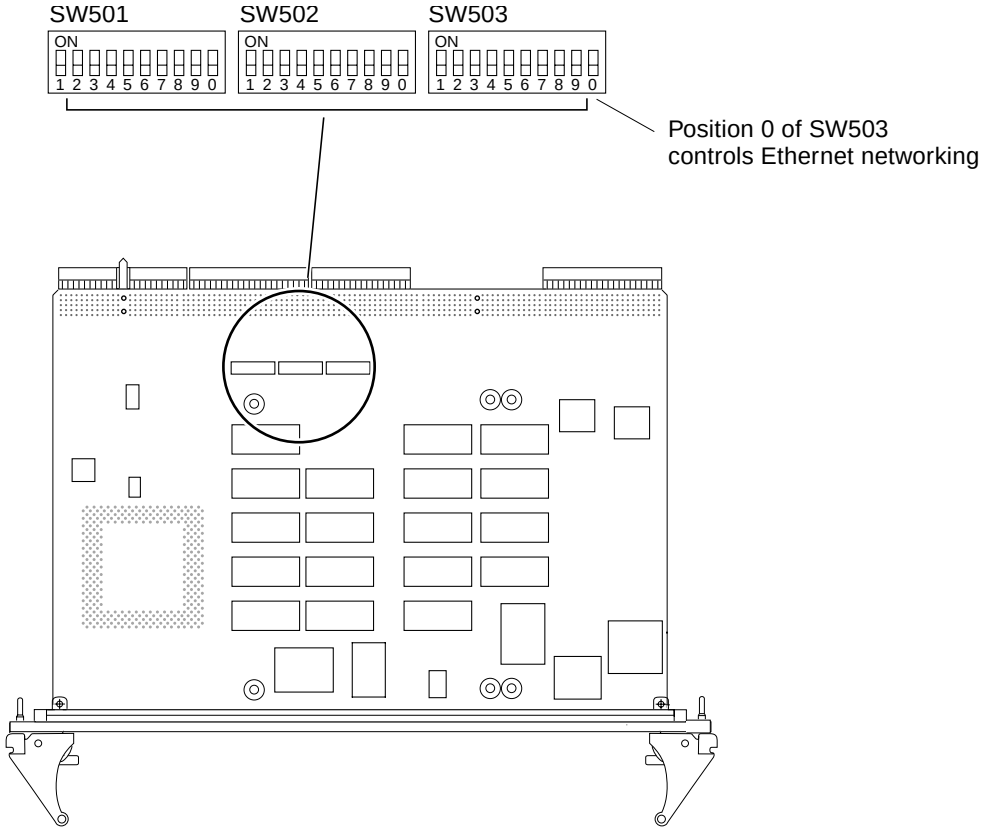

FIGURE B-5 Location and Default Settings of the SW501, SW502, and SW503 DIP Switches

Position 0 of SW503 controls the Ethernet networking on the Netra CP2300 board and transition card. By default, position 0 is set to OFF, which means that the board is set for cPSB network mode and the Netra CP2300 transition card's RJ45 Ethernet ports are disabled. If you will use the Netra CP2300 board in a non-cPSB enclosure, you should set Position 0 of SW503 to ON, so that you can use the RJ45 Ethernet connectors on the transition card.

The remaining DIP switch positions (SW501, 1 to 0; SW502, 1 to 0; SW503, 1 to 9) control the EIDE connector on the Netra CP2300 transition card. When these positions are set OFF, you will not be able to use the transition card's EIDE connector. In this setting, however, all of the pin signals (PIM_A_IO_1 to PIM_A_IO_64) on the PIM A Jn4 connector will be available. (The PIM A Jn4 connector is labelled J5 on the transition card.) See FIGURE B-6 for the location of the PIM A Jn4 (J5) and EIDE connectors. Refer to the *Netra CP2300 cPSB Transition Card Installation and Technical Reference Manual* (816-7188-*xx*) for the pin descriptions of these connectors.

When these DIP switch positions are set to ON, the EIDE connector on the transition card will be available. However, pins 1 through 29 on the PIM A Jn4 (J5) connector (PIM_A_IO_1 to PIM_A_IO_29) are disabled and *must not* have PIM A I/O connections.

TABLE B-15 SW501, SW502, SW503 DIP Switch Settings

DIP Switch, Position Numbers	Default Setting	Description
SW501, positions 1 to 0 SW502, positions 1 to 0 SW503, positions 1 to 9	OFF	Controls the EIDE and PIM A J5 connectors on the Netra CP2300 transition card. • OFF = EIDE connector disabled and PIM A J5 connector enabled • ON = EIDE connector enabled and PIM A Jn4 (J5) connector pins 1 through 29 disabled
SW503, position 0	OFF	Controls the RJ45 Ethernet connectors on the Netra CP2300 transition card. • OFF = cPSB network mode; RJ45 Ethernet connectors disabled • ON = RJ45 Ethernet connectors enabled

Note – Even if you are not using the PIM_A_IO connections for transition card PIM applications, the PMC A slot restricts the use of PMC cards with PIM capability. If the PMC card uses the PIM_A_IO_1 to PIM_A_IO_29 signals, refer to your PMC card documentation to determine compatibility.

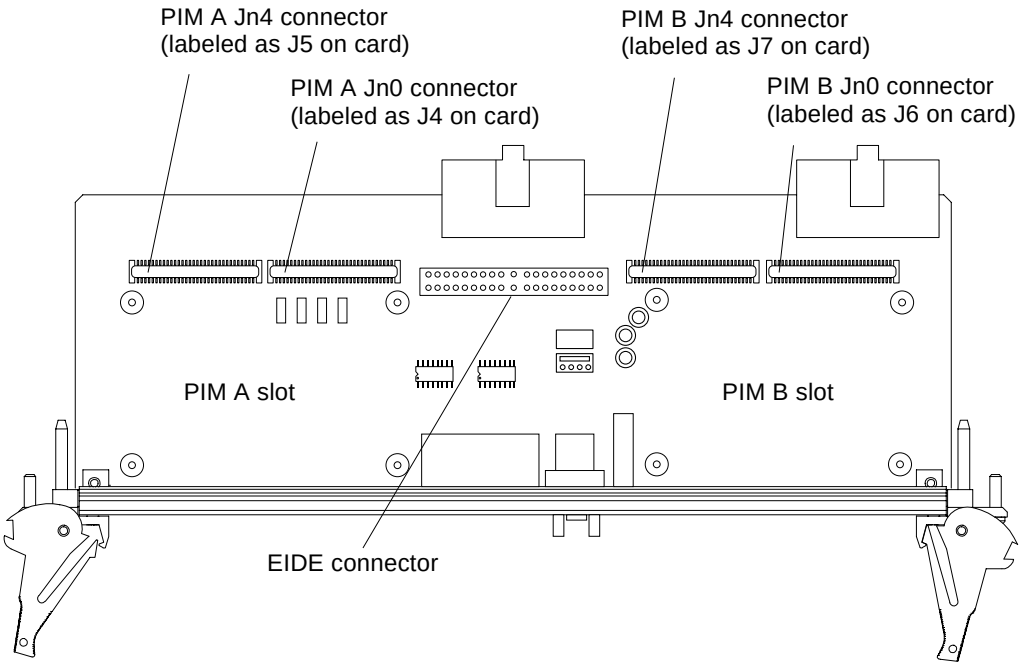

FIGURE B-6 Netra CP2300 cPSB Transition Card EIDE and PIM Connector Locations

APPENDIX **C**

Solaris Sun FRU ID

The Solaris Sun FRU ID information is stored on a Netra CP2300 board EEPROM and is used to identify the board for service purposes. The Solaris Sun FRU ID is one of the standard features in the Solaris 8 2/02 operating environment and later compatible versions. The Netra CP2300 board software implements the Solaris Sun FRU ID for the netra CP2300 board, when used with Solaris 8 update 2/02 and later compatible versions.

To access the Solaris Sun FRU ID information for a board, use the `prtfru` command. See the `prtfru(1M)` man pages for further information on this command. The man pages can be found on the Solaris 8 2/02 operating environment default package and on the Solaris documentation web site:

`http://docs.sun.com/`

C.1 `prtfru` Command

By typing in the `prtfru` command at the Solaris command line, the user can obtain an output with Solaris Sun FRU ID information that is similar to the output shown in the following code example. The fields that are displayed in the example are described below in TABLE C-1.

```
# prtfru
/frutree
/frutree/chassis (fru)
/frutree/chassis/CPU-slot?Label=CPU
/frutree/chassis/CPU-slot?Label=CPU/CPU-slot (container)
   SEGMENT: SD
      /ManR
      /ManR/UNIX_Timestamp32: Fri May 11 19:00:00 PDT 2002
      /ManR/Fru_Description:
      /ManR/Manufacture_Loc:
      /ManR/Sun_Part_No: 375-302
      /ManR/Sun_Serial_No: 001379
      /ManR/Vendor_Name: Sun Microsystems
      /ManR/Initial_HW_Dash_Level:
      /ManR/Initial_HW_Rev_Level:
      /ManR/Fru_Shortname: CP2300
/frutree/chassis/CPU-slot?Label=CPU/CPU-slot/c0?Label=c0
#
```

TABLE C-1 Description of Fields in Typical `prtfru` Command Display Output

Field	Description
`/ManR/UNIX_Timestamp32: Fri May 11 19:00:00 PDT 2002`	Board manufacturing timestamp
`/ManR/Fru_Description:`	Description for the board field replaceable unit
`/ManR/Manufacture_Loc:`	Location where board is manufactured
`/ManR/Sun_Part_No: 375-302`	Board identification part number
`/ManR/Sun_Serial_No: 001379`	Board identification serial number
`/ManR/Vendor_Name: Sun Microsystems`	Name of the board vendor
`/ManR/Initial_HW_Dash_Level:`	Board identification dash number
`/ManR/Initial_HW_Rev_Level:`	Board identification revision number
`/ManR/Fru_Shortname: CP2300`	Short name for the board such as CP2300

APPENDIX **D**

Bibliography

D.1 General References

The following books and specifications are referenced that relate the Netra CP2300 design.

D.1.1 Books and Specifications

PCI Special Interest Group.*PCI Local Bus Specification, Revision 2.1.* Available at `http://www.pcisig.com`. Portland, OR. June 1995.

PCI Special Interest Group.*PCI Hot-Plug Specification, Revision 1.0.* Available at `http://www.pcisig.com`.Portland, OR.

PCI Industrial Computers Manufacturers Group. *CompactPCI Specification, PICMG 2.0 R3.0,* October 1999.

PCI Industrial Computers Manufacturers Group. *CompactPCI Specification Short Form, PICMG 2.0 R2.1*, September 1997.

PCI Industrial Computers Manufacturers Group. *CompactPCI Hot Swap Specification, PICMG 2.1 R1.0*, Wakefield, MA, August 1998.

CompactPCI Multi Computing Specification, PICMG 2.14; This reference covers several documents presently in draft form

PCI Industrial Computers Manufacturers Group. *CompactPCI Packet Switching Backplane specification, PICMG 2.16 R 1.0*, September 2001

CompactPCI Computer Telephony Specification, PICMG 2.5 R1.0, April 1999.

PCI Industrial Computers Manufacturers Group. *CompactPCI Power Interface Specification, PICMG 2.11 R1.0*, October 1999.

PCI Industrial Computers Manufacturers Group. *PMC on CompactPCI Specification, PICMG 2.3 R1.0*. August 1998.

PCI Industrial Computers Manufacturers Group. *CompactPCI 6U Dual System Slot Specification, PICMG 2.7*

PCI Industrial Computers Manufacturers Group. *IP on CompactPCI Specification, PICMG 2.4 R1.0*. August 1998.

PCI Industrial Computers Manufacturers Group. *PCI-PCI Bridge Board Connector for Single Board Computer, PICMG 1.1 R1.0*

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PCI Industrial Computers Manufacturers Group. *Keying of CompactPCI Boards and Backplanes, PICMG 2.10 Draft 0.4*, September, 1998.

Enterprise Computer Telephony Forum, *H110 Hardware Compatibility Specification: CT Bus, Revision 1.0*. 1997.

Intel Corporation, Hewlett Packard Company, NEC Corporation, Dell Computer Corporation. *Intelligent Platform Management Interface Specification, v1.0, Document Revision 1.1*. August 1999.

Intel Corporation, Hewlett Packard Company, NEC Corporation, Dell Computer Corporation. *Intelligent Chassis Management Bus Bridge Specification, v1.0, Document Revision 1.00*. August 1999.

Bureau Central de la Commission Electrotechnique Internationale. *EuroBoard Specification, IEC 297-3 and -4*. Geneva, Switzerland.

International Electrotechnical Commission, American National Standards Institute, *Draft Specification for 2 mm Connector Systems, IEC-61076-4-101*. New York, NY.

IEEE, *Draft Standard for a Common Mezzanine Card Family: CMC, P1386 Draft 2.1*, New York, NY. Oct. 1999. Covers mechanical specifications for PMC cards.

VITA Standards Organization. *PMC I/O Module Standard, VITA 36, 199X, Draft 0.1*, Scottsdale, AZ. July 1999. Gives mechanical definition and contact assignments for PIM cards.

Institute of Electrical and Electronics Engineers, Inc. Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards PMC, P1386.1 Draft 2.1. New York, NY. October 1999. Covers electrical specifications and contact assignments for PMC cards.

Institute of Electrical and Electronics Engineers, Inc. *IEEE Standard for Mechanical Rear Plug-in Units Specifications for Microcomputers Using IEEE 1101.1 and IEEE 1101.10 Equipment Practice, IEEE Std 1101.11-1998*. New York, NY. 1998. ISBN 0-7381-0179-6

Institute of Electrical and Electronics Engineers, Inc. *IEEE Standard for Mechanical Core Specifications for Microcomputers Using IEC 603-2 Connectors, IEEE 1101.1-1991*, New York, NY.

Institute of Electrical and Electronics Engineers, Inc. *IEEE Standard for Additional Mechanical Specifications for Microcomputers Using the IEEE Std 1101.1-1991 Equipment Practice, IEEE Std. 1101.10-1996*. New York, NY. 1997. ISBN 1 55937-863-8

Institute of Electrical and Electronics Engineers, Inc.*IEEE Standard for Additional Mechanical Specifications for Microcomputers using IEEE 1101.1 Equipment Practice, IEEE 1101.11*. Piscatowany, NJ.

Institute of Electrical and Electronics Engineers, Inc.*IEEE Standard: Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990*. New York, NY. 1990.

Institute of Electrical and Electronics Engineers, Inc. *IEEE Standard: Telecommunications and Information Exchange Between Systems--Local and Metropolitan Area Networks--Specific Requirements--Part 3: Carrier Sense Multiple Access With Collision Detection (CSMA/CD) Access Method And Physical Layer Specifications, IEEE Std 802.3–1998*. New York, NY. 1998. (This edition includes all contents of the 8802-3:1996 Edition, plus IEEE Std 802.3aa-1998, IEEE Std 802.3r-1996, IEEE Std 802.3u-1995, IEEE Std 802.3x&y-1997, and IEEE802.3z-1998).

Linear Technology LTC1643L/LTC1643H PCI-Bus Hot Swap Controller, September 1998

Dallas Semiconductor. *DS80CH11 System Energy Manager Product Specification, V2.0 15*.

Dallas Semiconductor. *High-Speed Microcontroller User's Guide*.

Philips Semiconductors. *I2C Peripherals Data Handbook IC12*. 1997.

Shanley, Tom, and Don Anderson andMindshare, Inc. *PCI System Architecture*, 4th ed., Reading MA: Addison Wesley, 1999

Solari, Edward, and George Willse. *PCI Hardware and Software Architecture and Design*. San Diego: Annabooks, 1998.

D.2 Sun Microsystems Publications

These books and papers are available in printed form, and some are also available through the World Wide Web.

You can browse the Sun documentation archive or search for a specific book title or subject.

`http://www.sun.com/documentation`

D.2.1 Solaris Operating Environment

Note – To locate documentation for future compatible versions of the Solaris operating environment, refer to Solaris documentation web site: `http://docs.sun.com`.

Solaris 8 (SPARC Platform Edition) Installation Guide, Part No. 806-0955-*xx*

Solaris 8 Advanced Installation Guide, Part No. 806-0957-*xx*

Solaris 8 System Administration Supplement, Part No. 806-6611-*xx*

System Administration Guide, Volume 1, Part No. 805-7228-*xx* (contains chapters on device management and configuring devices—presently deals with hot- plug considerations).

System Administration Guide, Volume 2, Part No. 805-7228-*xx* (of general interest)

System Administration Guide, Volume 3, Part No. 805-7228-*xx* (of general interest)

man pages section 1M: System Administration Commands, Part No. 806-0625-*xx* (covers `cfgadm` command; see above discussion on hot-swap support in the reference to the *System Administration Guide, Volume 1*.)

OpenBoot 4.x Command Reference Manual, Part No. 816-1177-*xx*

Writing FCode 3.x Programs, Part No. 806-1379-*xx* February 2000, Rev

OpenBoot 3.x Quick Reference, Part Number 806-2908-10, February 2000, Revision A

Solaris Naming Administration Guide, Part No. 806-1387-*xx*

Solaris Naming Setup and Configuration Guide, Part No. 806-1386-*xx*

Writing Device Drivers, Part No. 805-7378-*xx* (includes information about the device tree)

D.2.2 Alternate Pathing

These documents can be read for an approximation of the installation procedure that will apply to the CP2000 HA platform.

Sun Enterprise Server Alternate Pathing 2.3 User Guide, Part No. 806-1933-*xx*

Sun Enterprise Server Alternate Pathing 2.3 Reference Guide, Part No. 806-1934-*xx*

D.2.3 SunVTS System Exerciser

SunVTS 4.0 Users Guide, Part No. 806-2057-*xx*

SunVTS 4.0 Test Reference Manual, Part No. 806-2058-*xx*

D.2.4 Netra CP2300 Board Documents

You can find other Netra CP2300 board manuals, as well as the other Netra CPU board documentation, at the following web site:

`http://www.sun.com/products-n-solutions/hardware/docs/CPU_Boards`

Glossary

The terminology used in this glossary conforms to PICMG and Telco industry terminology.

Glossary Listing

Alternate Pathing (AP) A software-driven facility that employs both redundant hardware and redundant software driver paths between a server and a disk subsystem or a network. If one path fails, AP can ensure that the disk subsystem or network is still available through the alternate path. For example, the alternate path can be a second port on an interface board, or an entirely separate interface board. See also Dynamic Reconfiguration.

availability The ratio of the total time that a functional unit can be used to the total time that the unit is required for use.

Baseboard Management Controller (BMC) Manages chassis environmental, configuration and service functions and receives event data from other parts of the system. It can receive data through sensor interfaces, and interprets these data by using the sensor data repository (SDR) to which it provides an interface. The BMC maintains and provides an interface to the system event log (SEL). The BMC allows both the SDR and the SEL to be accessed from the system or from the intelligent platform management bus (IPMB). A typical function of the BMC is to measure processor temperature, power supply values, and cooling fan status. It can take some autonomous actions to preserve system integrity. For example, it might switch on a fan at a particular temperature threshold. An application interface

may be provided to enable custom user-management applications to be built. The BMC describes an abstract function, or role. It carries no definition of how the role might be implemented.

checkpoint (1) A point at which information about the status of a job and the system can be recorded so that the job can later be restarted from that point. (2) A sequence of instructions in a computer program for recording the status of execution for restarting.

CompactPCI (cPCI) An adaptation of the PCI bus architecture defined in the *Peripheral Component Interconnect Specification 2.1* (or later) to an electrically-compatible robust industrial form. This form specifies an Eurocard-style circuit board assembly that uses "hard metric" connectors to connect it to the enclosure backplane. CompactPCI is an open specification supported by the PCI Industrial Computers Manufacturers' Group (PICMG).

CompactPCI bridge The PCI bridge between the system host processor and the CompactPCI bus. The CompactPCI bridge must reside in the system slot to provide CompactPCI clocking and arbitration that are only available from that slot. CompactPCI Bridges must be controllable by the system management controller to turn off clocks and arbitration.

Device Reconfiguration (DR) A process that is used in the CP2000 system to configure (add) or deconfigure (remove) device tree allocations and load or unload software driver modules while the system is running. It is analogous to *Dynamic Reconfiguration* that is used on some Sun high-end server systems with the important differences: it is not used to reconfigure memory or CPU resources and it can be used automatically in the full hot-swap and HA hot-swap cases when the hot-swap framework software is prompted by the System Management Controller. CP2000 HA device reconfiguration can also be invoked manually from a console.

domain That part of a computer network in which the data processing resources are under common control. See *PCI Domain*.

drop-in A drop-in is a code or data module that can be called by the OpenBoot PROM during system startup. It is placed in unused memory space between OpenBoot PROM and OpenBoot PROM. Most user-created drop-ins are used to initialize custom user hardware. They do not require that the user possesses OpenBoot PROM source code; only the binary OpenBoot PROM image need be licensed. Drop-ins are used to add firmware drivers for user hardware.

Dynamic Reconfiguration (DR) A software package that enables the administrator to (1) view a system configuration; (2) suspend or restart operations involving a port, storage device, or board; and (3) reconfigure the system (detach or attach hot-swappable devices such as disk drives or interface boards) without the need to power down the system. When DR is used with Alternate Pathing or Solstice

DiskSuite software (and redundant hardware), the server can continue to communicate with disk drives and networks without interruption while a service provider replaces an existing device or installs a new device. DR supports replacement of a CPU/memory board, provided the memory on the board is not interleaved with memory on other boards in the system. Note that DR is used with Sun high-end server systems. See *Device Reconfiguration* for the analogous process that is applied to CP2000-based systems.

environmental monitoring The provision of hardware status information to the user or application program to enable an orderly shut down to be made before a hardware failure causes any damage.

failover The transfer of function from a failed component subsystem to an alternate one while preserving the operational state of the overall system. The functions transferred may include those of control and management.

firmware An ordered set of instructions and data that is stored in a way that is functionally independent of main storage, for example, microprograms stored in a read-only memory (ROM). The term *firmware* describes microcode in ROM. At the time they are coded, microinstructions are software. When they are put into ROM they become part of the hardware (microcode) or a combination of hardware and software (microprograms). Usually, microcode is permanent and cannot be modified by the user.

Field Replaceable Unit (FRU) A part or subsystem that may be replaced in the field or at a customer-site. Parts that are not FRUs are only factory replaceable.

Gigabit Media-independent Interface (GMII) An Ethernet network specification that defines a standard 1000-megabit interface between the MAC layer and either of the physical layers: 1000BASE-X (fiber-channel family) or 1000BASE-T (UTP). The GMII accommodates these physical layers without having to modify the upper layers (that is, the protocol stacks) for the particular transmission medium. The GMII is defined in IEEE Std. 802.3z–1998, which is included in IEEE Std. 802.3–1998.

handover Synonymous with *switchover.* The transfer of function from a component subsystem to an alternate one while preserving the operational state of the overall system. The functions transferred may include those of control and management. Handover occurs when there is no failure in the system to prompt the transfer (compare *failover).*

heartbeat A repetitive signal passed from one system to another to communicate the state of integrity or “health” of the sending system.

High Availability (HA) The property of a system associated with a high in-service to out-of-service time ratio. This property can be engineered by reconfiguring the system "on the fly" to isolate failed elements so they can be replaced without affecting the operational condition.

host computer (1) A computer that usually performs network control functions and provides end-users with services such as computation and database access.

(2) The primary or controlling computer in a multicomputer installation.

hot-plug A slot must be powered down and isolated from the bus before an adapter card can be inserted. The hot-plug specification requires that board power be controlled and that means be provided to set or maintain the board in a quiescent state prior to its insertion or removal.

The method of putting the board in a quiescent state or of controlling power application to it is not defined in hot-plug but is left to the system manufacturer. The hot plug interface is defined by the PCISIG—see the hot-plug specification in the Bibliography.

hot-swap The ability of a system element to be removed or replaced while the system hardware is nominally operating under power. This ability is usually invoked after a failure and is implemented by a sequence that steers the functions of the element to other parts of the system.

Hot-swap, as defined by PICMG, can be classified as basic, full, or HA. Basic hot-swap requires manual software sequencing to bring a card out of commission. Full hot-swap uses hardware enumeration signals to indicate board status. Software automatically decommissions the card. HA hot-swap provides for a fully automated decision tree and use of software and a System Management Controller / Hot-Swap Controller to decommission or commission a card.

hot-swap controller The controller that takes care of the low-level sequencing associated with hot-swap.

Inter-Integrated Circuit Bus (I^2C) A serial bus developed by Philips for inter-package communications and typically used by them in TV sets. In Sun CompactPCI systems, it is used to link card elements in a system for management communications.

Inter-Chassis Management Bus (ICMB) An IPMI / I^2C bus (analogous to the IPMB) used to accomplish chassis-to-chassis management.

Inter-Host Bus (IHB) An IPMI / I^2C bus (the IPMB) used for direct communications between controllers on host boards.

Input/output (I/O) Applies to system peripheral signals.

Intelligent platform management bus (IPMB) A bus that carries serial communication signals that comply with the IPMI; it is used to communicate between CompactPCI circuit boards in a chassis.

Intelligent Platform Management Interface (IPMI) A protocol interface with a protocol stack that includes link, transport, and session layers to provide reliability. IPMI resides on an I^2C physical layer.

Keyboard Control Style interface (KCS interface) One of the BMC to System Management Software (SMS) interfaces as defined in the IPMI specification (see the Bibliography).

LVD SCSI A version of the SCSI bus that uses LVTTL (3.3 V) differential logic technology. This bus is currently specified with an 80 MHz maximum transfer rate and a maximum cable length of 18 ft.

Medium Access Control (MAC Address) Synonymous with Ethernet address. The MAC address is a 48-bit address used to direct data-link layer transactions.

Media-Independent Interface (MII): A specification that defines a standard interface between the MAC layer and any of the three physical layers: 100BASE-TX, 100BASE-T4, or 100BASE-FX. It can support both 10 Mbps and 100 Mbps data rates. Since the electrical signals are clearly defined, the MII may be implemented internally or externally in a network device.

nexus A nexus driver supports a bridging connection for communication between devices on separate buses. These devices can be arranged in a hierarchal tree configuration with a number of bridges. In this case a nexus driver is associated with each bridge to handle communications with adjacent levels in the hierarchy.

nines Used as a measure of system availability: three nines > 99.9% availability, four nines > 99.99%, five nines > 99.999%; six nines > 99.9999%;...

Non-maskable interrupt (NMI) An interrupt that cannot be ignored. An NMI is issued for serious conditions that demand the processor's immediate attention.

Node An addressable point on a network. Each node in a Sun network has a different name. A node can connect a computing system, a terminal, or various other peripheral devices to the network.

OpenBoot PROM (OBP) The OpenBoot PROM, or system PROM, contains code to run POST and a suite of user-accessible subsystem hardware tests. It has a Forth interpreter for custom user routines. Under a normal boot sequence, it provides a path to a system boot device which is accessed after POST completes. “Open Firmware” is defined by IEEE Standard 1275.

PCI domain The functional entity that includes a host—usually with a host PCI bridge—and the peripherals that it controls. The domain does not necessarily uniquely include the PCI bus because this bus can be shared by multiple domains. For example, a second domain can comprise a second host/bridge element that controls a different set of peripherals on a shared bus. Separation and management of the domains is implemented by a controlling system mechanism that guarantees their mutual protection.

peripheral host See *satellite host*

PICMG PCI Industrial Computers Manufacturers’ Group.

PCI Mezzanine Card (PMC) A PMC card fits into a special PCI-bus connector designed to attach compact peripherals. These peripherals may decode a variety of I/O functions from this bus.

Power-On Self Test (POST) A suite of tests run out of system firmware before any other code is loaded. The purpose of such testing is to check the integrity of the hardware before loading a software system.

Reverse Address Resolution Protocol (RARP) The protocol broadcasts a MAC (ethernet) address and receives an IP address in response from a RARP server.

Reliability, Availability and Serviceability (RAS) The general concepts associated with high in-service time systems and their simplicity of maintenance.

reliability The ability of a functional unit to perform a required function under stated conditions for a stated period of time.

remote management The action of managing a system or group of systems from a physically distant location. Remote management of Sun systems may be performed using the *Sun Management Center* application.

satellite board See *satellite host*.

satellite host Synonymous with *peripheral host* and *satellite board*. A satellite host performs independent tasks in response to commands from the system host. The satellite host has no accessible PCI space and is limited to controlling its own on-board I/O.

sensor data repository (SDR) The database that the BMC uses to determine what sensors, FRU devices, and management controllers are in the system. This database contains an account of sensor locations, properties, and associations.

segment The extent to which a backplane and cards combination can be extended by accounting for signal loading. In CompactPCI, a segment spans a maximum of eight card slots, beyond which some bridge elements (system bridge) are needed to provide expansion into another segment.

system event log (SEL) The database of measured values and events that is created by the BMC based upon its sensor monitoring. This database resides in the host and is accessible by high-level applications.

serviceability The capability of performing effective problem determination, diagnosis, and repair on a data-processing system.

shelf A single physical computing system composed of one or more CompactPCI bus segments. Electrical limitations of the bridging interfaces may require that the segments be in close proximity.

switchover See *Handover.*

system board computer The processor board that connects to a backplane system slot.

system host A system host accepts interrupts and owns peripherals. It executes user applications and decides the distribution of tasks within a system. In Hot-Swap systems the system host acts as a traffic router and functions to activate and deactivate peripheral cards (plug-in boards). It is not a CompactPCI requirement that the system host reside in a system slot, although this is normally the case. If the board resides in a peripheral slot that slot must be wired to receive peripheral interrupts from the backplane.

system management bus A serial bus that carries data and control signals between System Management Controllers on peripheral boards and devices. Communications on this bus use the IPMI protocol over an I^2C hardware layer.

System Management Controller (SMC) There is a System Management Controller (SMC) on each card in the enclosure. One of these cards either assumes control by command or takes control after negotiation with the other System Management Controllers. The System Management Controller manages peripherals to improve the availability of the system. Through the IPMB, this entity receives information on IDs of, or problems with, cards in the system and can communicate that information with other cards or with a system host via another bus. The SMC can switch the PCI bridge, PCI arbitration, and PCI clocking on or off.

system slot The card location in an enclosure that provides for CompactPCI clocking and arbitration. The CompactPCI bridge, which supplies these functions, must be in the system slot.

system-slot bridge Provides clocks and arbitration. This device must be controllable from somewhere, including a controller. The system host need not reside on the same card but the card that performs the function of system host must be able to talk to the slot containing the system-slot bridge.

takeover See *failover.*

Trivial File Transfer Protocol (TFTP) A simplified form of File Transfer Protocol (FTP). It contains no password checking and is typically used to boot diskless workstations and other boot clients.

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